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32-Bit Vedic Alu with Low Power Mode

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Abstract- Power consumption and computational speed are important factors in modern digital systems. This project presents a 32-Bit Vedic ALU with Low Power Mode using System Verilog. The design employs the Urdhva Tiryakbhyam algorithm for fast multiplication and incorporates operand isolation and clock gating techniques to reduce power consumption. The ALU performs arithmetic, logical, and shift operations efficiently while maintaining high performance. The proposed system provides a high-speed, reliable, and power-efficient solution for embedded systems and processor applications.

Keywords: 32-Bit Vedic ALU, Vedic Mathematics, Urdhva Tiryakbhyam Multiplier, Vedic Divider, Low Power Mode, Operand Isolation, Clock Gating, System Verilog, Low Power VLSI Design, High-Speed Computation, Power Optimization, Arithmetic Operations, Logical Operations, Shift Operations.

I. INTRODUCTION

Arithmetic Logic Units (ALUs) are essential components of digital systems and processors. Conventional ALUs often face challenges related to power consumption and computational delay.

This project presents a 32-Bit Vedic ALU with Low Power Mode using System Verilog. The design utilizes the Urdhva Tiryakbhyam algorithm for fast multiplication and employs operand isolation and clock gating techniques to reduce power consumption.
The system provides a high-speed, reliable, and power-efficient solution for modern embedded and processor applications.

II. LITERATURE SURVEY

[1] Verma & Jain (2024):
The authors proposed an energy-efficient Vedic multiplier using the Urdhva Tiryagbhyam algorithm. Their results showed improved speed and reduced power consumption compared to conventional multipliers.

[2] FPGA-Based Comparison of Vedic and Array Multipliers (2025):
This study analyzed low-power ALU design using operand isolation techniques. The results demonstrated reduced switching activity and lower dynamic power dissipation.

[3] Tiwari (2025):
The author presented a high-speed Vedic ALU using optimized RTL design techniques. The architecture achieved improved computational performance with reduced power consumption.

[4] Kumar & Sharma (2023):
This paper introduced a high-speed Vedic divider based on the Paravartya Yojayet algorithm. The design provided faster division and efficient hardware utilization.

[5] Mehta & Joshi (2024):
The authors proposed a Vedic division architecture using Nikhilam and Paravartya techniques. The results demonstrated reduced delay and improved arithmetic performance compared to conventional division methods.

III. PROBLEM STATEMENT AND OBJECTIVES

Conventional ALUs consume unnecessary power because internal blocks such as the adder, logic unit, multiplier, and divider remain active even when they are not required. This project addresses the problem by designing a 32-Bit Vedic ALU with Low Power Mode using Vedic arithmetic techniques and power optimization methods.

1. To design and implement a 32-Bit Vedic ALU using System Verilog.
2. To perform arithmetic and logical operations using Vedic multiplication and division techniques.
3. To reduce power consumption using operand isolation and clock gating techniques.
4. To improve computational speed and energy efficiency for digital and embedded applications.

IV. DESIGN METHODOLOGY

The 32-Bit Vedic ALU with Low Power Mode is developed using System Verilog. The design consists of arithmetic blocks such as adder, subtractor, Vedic multiplier, and Vedic divider, along with logical and shift operation units.

The Urdhva Tiryakbhyam algorithm is used for multiplication, while Vedic division techniques are employed for division operations. A multiplexer selects the required operation based on the control signal. Low-power techniques such as operand isolation and clock gating are incorporated to reduce unnecessary switching activity and power consumption.

This methodology ensures high-speed computation while maintaining improved energy efficiency and reliability.

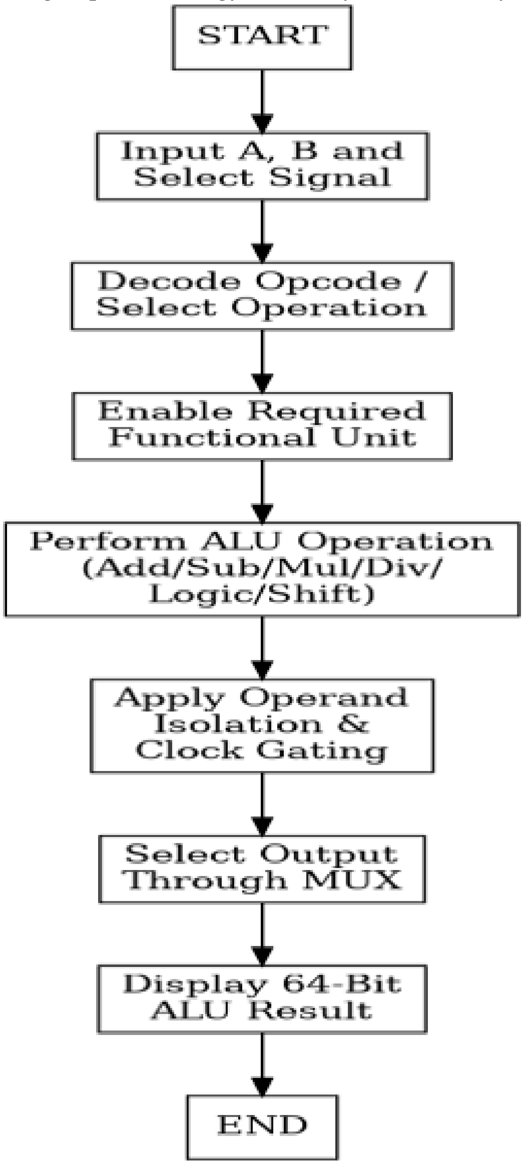

Figure 1: Flowchart of 32-Bit Vedic ALU with Low Power Mode

Block Diagram

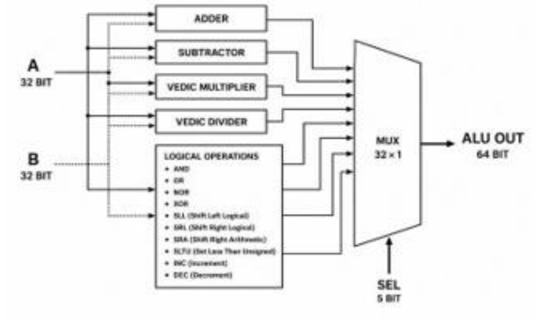

Figure 2: Block Diagram of 32-Bit Vedic ALU with Low Power Mode

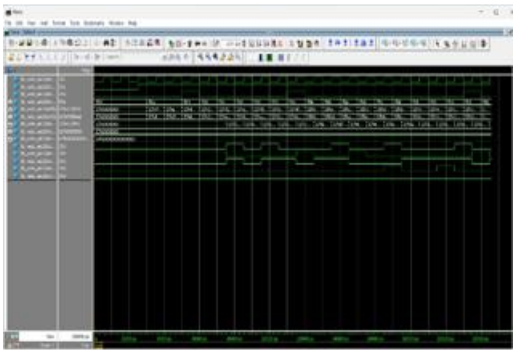

Figure 3: Result of 32-Bit Vedic ALU with Low Power Mode

V. RESULTS AND ANALYSIS

The proposed 32-Bit Vedic ALU with Low Power Mode was successfully designed, implemented, and verified using System Verilog. The architecture consists of arithmetic, logical, shift, multiplication, and division units integrated into a single ALU framework. Functional verification was carried out using a System Verilog testbench, and the simulation results confirmed the correct execution of all operations for various input combinations.

The arithmetic unit successfully performed addition and subtraction operations with accurate results. The Vedic multiplier, implemented using the Urdhva Tiryakbhyam algorithm, generated multiplication results efficiently through parallel partial product generation. Compared to conventional multiplication techniques, the Vedic approach reduced propagation delay and improved computational speed. Similarly, the Vedic divider based on Paravartya Yojayet and Nikhilam techniques performed division operations correctly while reducing computational complexity.

The logical operation unit successfully executed operations such as AND, OR, XOR, NOR, shift left logical (SLL), shift right logical (SRL), shift right arithmetic (SRA), increment, decrement, and SLTU operations. A multiplexer selected the required operation output based on the control signal, ensuring correct operation selection and output generation.

To improve energy efficiency, low-power techniques such as operand isolation and clock gating were incorporated into the design. These techniques prevented unnecessary switching activity in inactive functional units, thereby reducing dynamic power consumption. Only the functional block selected by the opcode remained active, while the remaining blocks were isolated from unnecessary signal transitions.

Simulation waveforms demonstrated the successful operation of all ALU functions under different test conditions. The results confirmed that the proposed design achieved a balance between high-speed computation and reduced power consumption. The integration of Vedic arithmetic techniques with low-power optimization methods enhanced overall ALU performance while maintaining design reliability.

The developed 32-Bit Vedic ALU with Low Power Mode provides an efficient solution for modern processors, embedded systems, and digital signal processing applications.

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