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Future ready Low-power 4-bit multiplier for portable VLSI systems

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Abstract- A multiplier is an essential part of many extremely large scale integration systems and finds extensive application in digital circuits for innumerable arithmetic calculations. One of the most fundamental operations in digital technology is multiplication, and hardware multipliers are essential for quick computing and efficient data processing. There have been several design approaches to multipliers that focus on surface area and energy efficiency in response to the desire for high-performance, low-power multipliers. Our study presents a 4-bit field multiplier with improved energy efficiency compared to conventional designs, using a modified gate-diffusion input (MGDI) cell architecture. The energy consumption of the MGDI-based multiplier is significantly reduced to 1.109861 mW without sacrificing any of the essential operating efficiencies. Thorough simulations have been conducted to showcase the performance of the 4-bit MGDI multiplier, which was meticulously constructed utilizing Tanner EDA tools. Low power, 4-bit multiplier, time delay, transistor count, modified gate diffusion input (MGDI) are some of the keywords.

Keywords- 4-Bit Multiplier, Low Power Design, MGDI Technique, Modified Gate Diffusion Input, VLSI Design, Energy Efficiency.

I. INTRODUCTION

There are a lot of good books that explain how to do multiple optimization. For the 8x8-bit multiplier employing CMOS SCN technology, the 3-bit encoding approach that is optimized for parallel multipliers using two-sided complement representation showed a latency of less than 5.7 ns [1]. Significant gains in structural uniformity and energy efficiency were achieved by the reconfigurable 8x8 wall wart multiplier, which was constructed using the 180 nm process that combined CMOS and GDI technologies [2]. By reducing power consumption and the amount of transistors, gate-diffusion input (GDI) technology has shown its adaptability in the 4-bit field multiplier [3]. Improving the power delay product was another step forward, achieved by combining a 4-bit field multiplier with a 10-transistor (10T) full-array accelerator [4].

However, the significance of energy-efficient design in portable devices has been highlighted by the integration of low-energy design strategies [5]. Using 10T complete amplifiers, 4x4-bit Dadda multipliers have considerably decreased the propagation latency, power consumption, and power delay product [6]. Using notions from Vedic mathematics, 4-bit Vedic multipliers based on GDI have achieved high speed and low power performance [7]. Simultaneously, better energy efficiency in mathematical processes has been shown using a novel low-power full-array amplifier that combines GDI with pass-through logic (PTL) [8]. Lastly, the Radix-8 high-speed binary multiplier was able to acquire the area, energy consumption, and time-to-life advantages by using the Urdhva-Tiryakbhyam and GDI approaches [9]. These innovations highlight how important it is for contemporary design to find a happy medium between speed, precision, and power.

Further, the use of FPGAs to create Vedic multipliers demonstrates the value of pipelines and parallelism in reducing latency and increasing throughput [10]. 4-bit multipliers are designed to be more energy efficient and produce less heat by using reversible logic gates [11]. Compared to complementary metal-oxide semiconductors (CMOS), field-effect transistors (FinFETs) for 8-bit multipliers operate faster and with less leakage energy [12]. By reducing the number of transistors and energy consumption, GDI has been effective in field multipliers [13]. By increasing the effectiveness of partial reductions, Wallace tree multipliers have increased both speed and energy efficiency [14]. The transmission gate logic has allowed for the development of low power multiplier designs, which are well suited for portable electronics [15].

II. OVERVIEW OF FULL ADDER

To perform the addition operation, a full-length adder logical circuit needs three binary digits, each of which is one bit. A carry-over output is produced by complete adders whenever two input values are added together. It is capable of operating independently as well as in combination with other full adders. Two one-bit binary outputs, the sum (S) and the carry (C1), are produced by the full-adder circuit from three one-bit binary values, namely C, A, and B. The cascade design relies on the carry-out from the previous circuit to initiate the carry-over to the full-adder circuit. Using the truth table as a starting point, the whole adder circuit is designed using the following input and output equations:

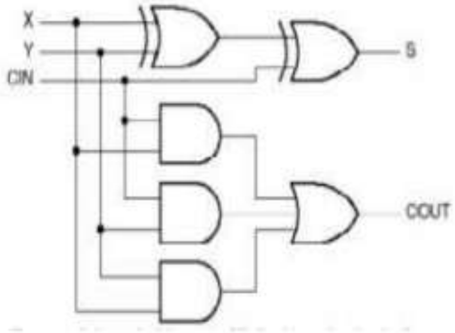

Fig. 1. Diagram of a 1-bit full adder block.

III. DESIGN METHODOLOGY

The fundamental cellular structures provide the basis of MGDI. The core cell looks like a regular CMOS inverter at first glance. But there's a big distinction.

1. NMOS and PMOS transistors have the same gate inputs. There are three inputs that are specified by the MGDI cell; one of them is p, which stands for PMOS source and drain input. The other two are nmos and mos, respectively. 2. While most of these functions are intricate in CMOS and conventional pass-through transistor logic (PTL) implementations, they are remarkably simple in multi-gate differential logic (MGDI) approaches, which only need two transistors for each function.

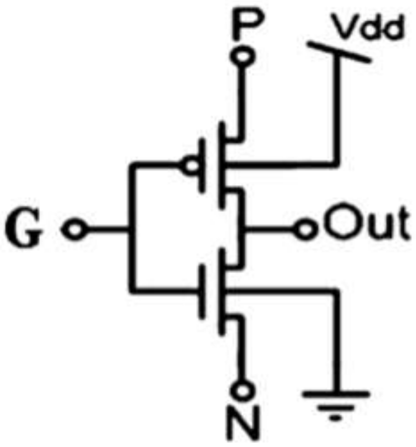

Fig. 2. MGDI basic cell

3. Three four-bit full complement gates and sixteen AND gates were used to create a four-by-four matrix multiplier. A 4x4 matrix multiplication factor is shown schematically in the following image. Reduced power consumption and a reduced number of transistors are the defining features of this architecture.

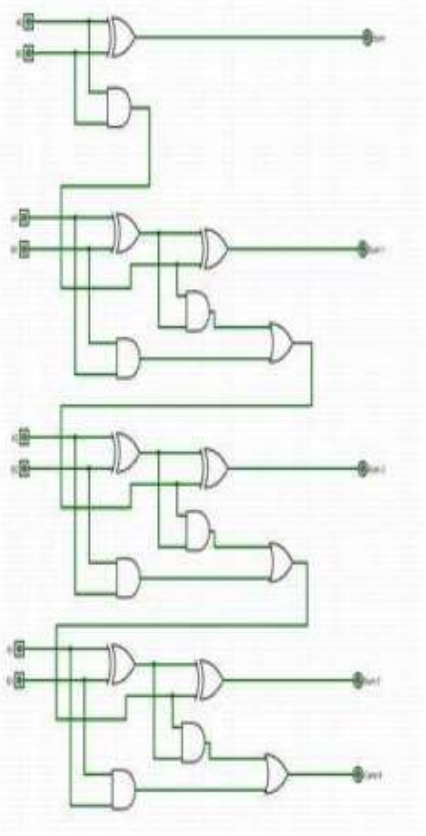

Fig. 3. Diagram of a 4-bit full adder block.

IV. PERFORMANCE PARAMETERS OF FULL ADDER

A. Power Dissipation

What we mean by "power dissipation" is the amount of energy that the full adder uses up and then "lost" while it's running. There are two main ways in which this energy loss is visible: Standing Power: This happens when the adder doesn't flip on but still uses energy from leakage currents (even when the transistors aren't turned on). When adding two numerical values, for example, the adder experiences dynamic power during state transitions. One reason for this is because every time an adder finishes a calculation, it must charge and discharge its internal capacitors.

Formula for Total Power Dissipation:

$$P_{\text{total}} = \alpha \cdot CL \cdot V_{DD}^{2} \cdot f + Isc \cdot V_{DD} + Ileak \cdot V_{DD} \tag{3}$$

B. Propagation Delay

It takes longer for the input signal to reach half of the exit level than the circuit spreads, according to this. C. PDP, or Power-Delay Product The Power-Delay Product is a unified quantitative metric that incorporates both power dissipation and propagation delay. This measure shows how much energy the adder uses for each operation cycle and how long it takes to complete that operation. Performance and energy efficiency are both improved with a lower PDP.

Formula:

$$PDP = P_{\text{total}} \times t_{pd} \tag{4}$$

V. SIMULATION RESULTS AND DISCUSSIONS

The full adder and the modified full adder are both built in the same manner. Both the arithmetic adder and the complete adder circuits are included in it. Substituting EX-OR gates for AND gates makes up the modified complete adder.

The building of a single-bit complete adder circuit using MOSFETs to improve the adder's performance is shown in Fig.4 and Fig.5. The adder utilizes 14 transistors for power and leakage. The 4T XOR gate, shown in Fig.4, is an integral part of an adder cell and is responsible for the basic addition operation of the cell. Comparable to a single half-adder cell in operation. The 14-transistor full adder cell made use of two 4-transistor XOR gates. In the past, XOR gates only needed eight MOSFETs, but now there are many other topologies available. Specifically, a 4T XOR gate was used to increase circuit density. Utilizing this XOR gate reduces overall adder size and total leakage.

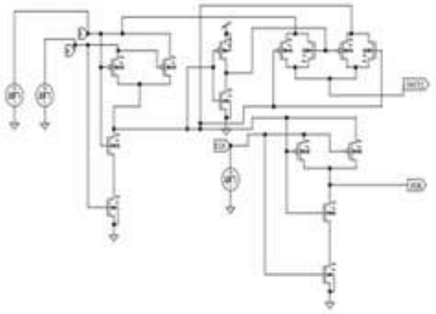

Fig. 4. 1-bit circuit diagram for normal GDI

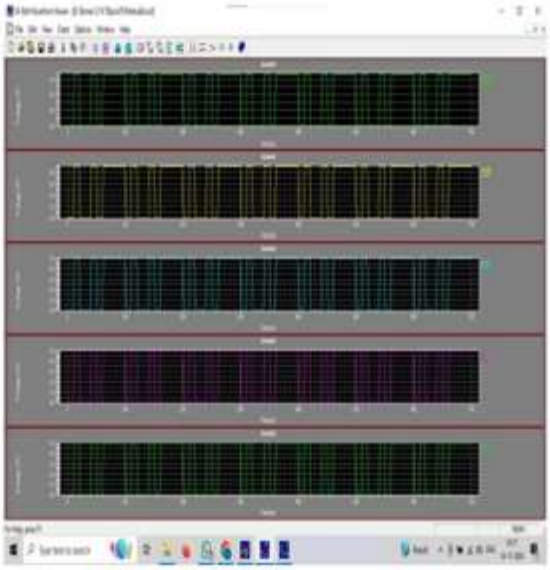

Fig. 5. Output waveform of GDI 1-bit full adder

Using a 10-transistor (10T) arrangement, the design of a single-bit full adder circuit is improved for performance and efficiency, as shown in Figures 6 and 7. The sum output in this design is generated using a 4T XOR gate, which uses a substantially less number of transistors than conventional XOR implementations. The XOR gate and efficient pass transistor logic for carry generation allow the circuit to accomplish all the necessary functions with only 10 transistors. Reduced power consumption, leakage, and total circuit size are achieved by this small design without sacrificing dependable operation.

Applications requiring low power and high density, where reducing transistor count while improving performance is paramount, are ideal for the 10T full adder.

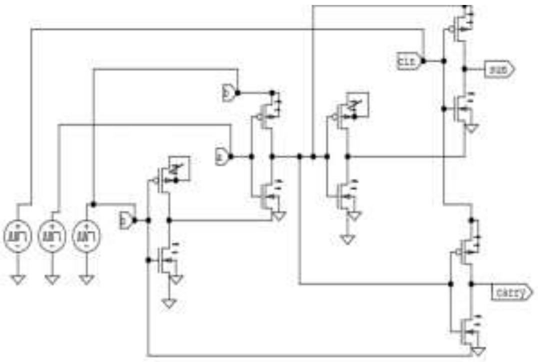

Fig. 6. 1-bit circuit diagram for MGDI

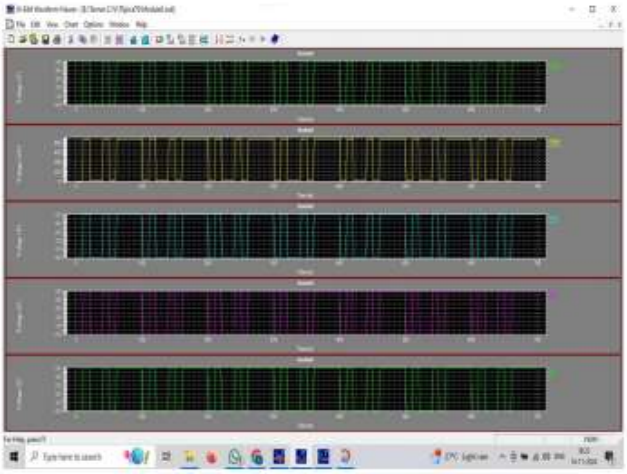

Fig. 7. Output waveform of MGDI 1-bit full adder

The Fig. 8 and Fig .9 are shows the 4-bit adder output of the above constraint parameter

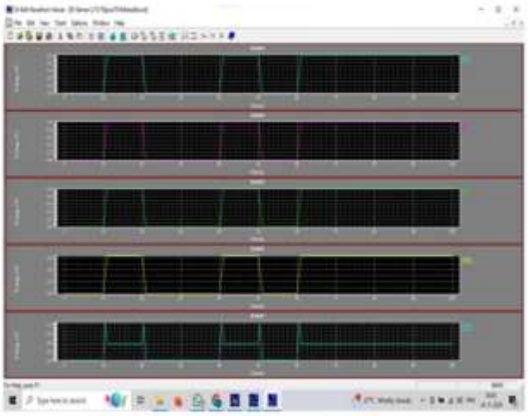

Fig. 8. Output waveform of GDI 4-bit full adder

TABLE I. COMPARISON BETWEEN 1-BIT FULL ADDERS

Types of logic	Conventional logic 1-Bit Full Adder	GDI 1-Bit Full Adder	MGDI 1-Bit Full Adder
No. of transistors	28	14	10
Power Consumption(mW)	3.347293	3.0615	1.4133
Delay (s)	0.19	0.17	0.05
Power-Delay Product (PDP)	0.6359	0.52046	0.070665

TABLE.It demonstrates that, on a number of important dimensions, the MGDI 1-bit full adder outperforms the GDI 1-bit full adder. Since the MGDI design only makes use of 10 transistors instead of the 14 used by GDI, it can fit into a smaller and maybe more cost-effective circuit.

In comparison to the GDI adder's 3.0615 mW, its power consumption rate is noticeably reduced, coming in at a modest 1.4133 mW. When it comes to modern digital circuit design, the MGDI 1-bit full adder is the way to go because of its improved efficiency, speed, and portability.

TABLE II. COMPARISON BETWEEN 4-BIT FULL ADDERS

Types of logic	Conventional logic 4-Bit Full Adder	GDI 4-Bit Full Adder	MGDI 4-Bit Full Adder
No. of transistors	416	56	40
Power Consumption(mW)	32.81	2.59117	1.108961
Delay (s)	0.39	0.31	0.12
Power-Delay Product (PDP)	12.7959	0.8032	0.133075

The MGDI 4-bit full adder outperforms the GDI 4-bit full adder in terms of operating efficiency and effectiveness, as shown in TABLE.II.

In addition, the MGDI adder is more suited for power-sensitive applications due to its reduced power consumption of 1.108961 mW compared to the GDI's 2.59117 mW. Better performance and faster processing are possible with the MGDI 4-bit full adder since its latency is 0.12 s, much lower than the GDI's 0.31 s. This is especially true for digital systems operating at high speeds. To sum up, modern digital circuit implementations may benefit from the MGDI 4-bit full adder's superior performance and efficiency.

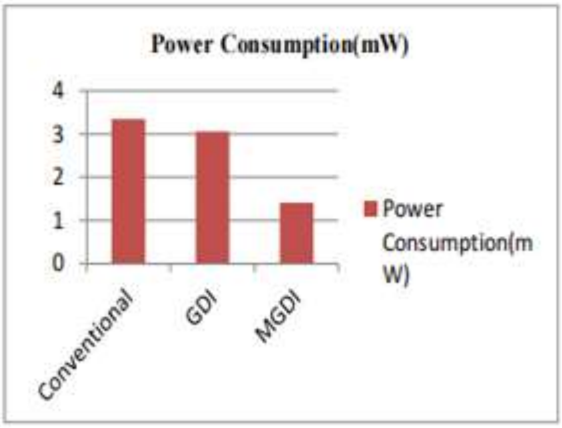

Fig.10. Comparison of power consumption (mW)

VI. CONCLUSION

Implementing a 4-bit multiplier employing MGDI (Modified Gate Diffusion Input) technology in the VLSI domain demonstrates minimal power consumption and time delay when compared to standard CMOS implementations. Due to its ability to reduce power consumption and chip area, MGDI is an excellent choice for low-power, high-efficiency VLSI circuits. This is particularly true for applications such as mobile processors, Internet of Things chips, and portable VLSI systems. Therefore, the suggested MGDI design significantly outperformed traditional logic, cutting power consumption by 57% and time delay by 73%. These results show that circuits that need to process information fast and with little power consumption may benefit from using MGDI technology., and it is a viable choice for energy-conscious VLSI designs of the future.

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