

Design and Implementation of Vedic Multiplier using Ripple Carry Adder Optimization

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Abstract- The Vedic Multiplier, derived from the ancient Urdhva-Tiryakbhyam sutra, provides an efficient and structured approach to perform high-speed multiplication, which is a fundamental operation in digital signal processing, image processing, embedded systems, and VLSI applications. Conventional multipliers such as array or Wallace tree multipliers, although accurate, often require large hardware resources and suffer from increased delay due to complex carry propagation paths, limiting their suitability for low-power and small-scale designs. In this project, a Vedic multiplier is designed and implemented in Verilog HDL, incorporating Ripple Carry Adder (RCA) optimization for the accumulation stage to reduce design complexity and ensure consistent performance. The design process covers the implementation of basic modules including AND, OR, Half Adder (HA), Full Adder (FA), and Ripple Carry Adder (RCA), which are then combined to form 2-bit and 4-bit Vedic multipliers. By leveraging the RCA for final addition, the architecture minimizes hardware overhead while maintaining reliable accuracy across test cases. Simulation and functional verification were carried out using industry-standard EDA tools, and results validate the correctness of multiplication operations for various inputs with low area utilization and moderate delay. The optimized Vedic multiplier demonstrates efficient trade-offs in terms of area and delay, establishing it as a simple yet effective solution for arithmetic-intensive applications in energy-constrained embedded systems and FPGA-based platforms, with scalability potential for higher bit-width multipliers. Furthermore, the simplicity of the RCA-based approach makes the proposed architecture highly adaptable for classroom learning, research, and prototyping environments where clarity and resource efficiency are essential. While advanced adders such as Carry Lookahead or Carry Save adders may provide lower propagation delay in large-scale multipliers, the Ripple Carry Adder offers a favourable balance of low power consumption, reduced complexity, and straightforward implementation, making it especially effective for small-to-medium bit-width operations. This highlights the practicality of the proposed design as a baseline for further optimization, with the potential to extend towards pipelined or parallel Vedic multiplier architectures suitable for real-time signal processing and embedded computing applications.

Keywords – Vedic Multiplier Urdhva-Tiryakbhyam Sutra Verilog HDL Ripple Carry Adder (RCA) Digital Signal Processing (DSP).

I. INTRODUCTION

Multiplication is a fundamental operation in digital systems and is widely used in digital signal processing (DSP), image processing, embedded systems, and VLSI applications. Conventional multiplier architectures such as Array, Booth, Wallace, and Dadda multipliers provide accurate results but involve complex carry-propagation paths, resulting in increased delay, higher power consumption, and significant hardware utilization. With the advancement of nano-scale technologies and the growing demand for portable and energy-

efficient systems, there is a need for compact and low-power multiplier designs.

Vedic mathematics, derived from ancient Indian computational techniques, offers efficient algorithms for arithmetic operations. Among these, the Urdhva-Tiryakbhyam (Vertically and Crosswise) sutra is well suited for digital multiplier design due to its ability to generate partial products in parallel, thereby improving speed and structural regularity. This makes Vedic multipliers a promising alternative to conventional architectures.

The motivation for this work is to design a multiplier that achieves a balance between performance, area, and power consumption. While high-speed adders such as Carry Lookahead Adders (CLA) reduce delay, they increase design complexity and hardware cost. In contrast, the Ripple Carry

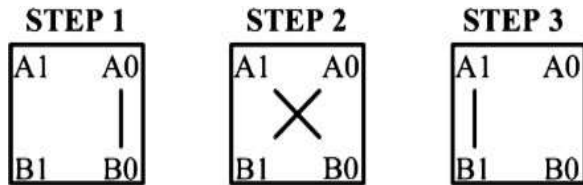


Fig.1 Vedic Multiplication using Urdhvaka Triyakbhyam

Adder (RCA) offers a simple and area- efficient solution, making it suitable for FPGA and small-scale VLSI implementations. Additionally, the growing use of multipliers in real-time applications such as filtering, encryption, and machine learning further emphasizes the need for optimized architectures.

In this paper, a Vedic multiplier optimized using a Ripple Carry Adder is proposed. The design combines the parallelism of the Urdhva-Tiryakbhyam sutra with the simplicity of RCA to achieve reduced hardware complexity and power consumption while maintaining acceptable performance. Unlike transistor-level optimization techniques such as Modified Gate Diffusion Input (m-GDI), which require specialized design environments, the proposed approach focuses on behavioral- level implementation, ensuring ease of design and scalability.

Objective

The novelty of this work lies in the integration of the Urdhva-Tiryakbhyam- based Vedic multiplier with a Ripple Carry Adder (RCA) at the architectural level to achieve an efficient balance between performance and hardware simplicity. Unlike existing approaches that focus on high-speed adders or transistor-level optimizations such as Modified Gate Diffusion Input (m-GDI), the proposed design emphasizes a behavioral-level optimization that significantly reduces area and power without increasing design complexity.

Furthermore, this work demonstrates that for small-to-medium bit-width multipliers, the use of RCA provides a practical and resource- efficient alternative to complex adder structures, making the design highly suitable for FPGA-based and low-power embedded applications. This combination of algorithmic efficiency and architectural simplicity distinguishes the proposed approach from conventional and existing Vedic multiplier designs.

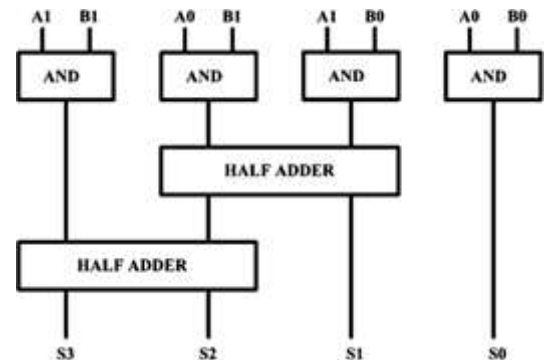


Fig.2. 2-bit Vedic Multiplier using Half Adders.

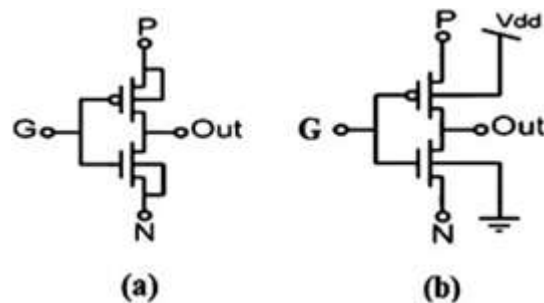


Fig.3. Basic GDI cell (b) Modified GDI (m-GDI) cell.

II. RELATED WORKS

Vedic multipliers based on the Urdhva- Tiryakbhyam sutra have been widely adopted for high-speed arithmetic operations due to their inherent parallelism and reduced computational delay. Early work by Himanshu Thapliyal and M. B. Srinivas (2014) demonstrated improved performance of Vedic multipliers over conventional array multipliers in FPGA implementations.

Subsequent studies, including R. Poornima and B. Priyadarshini (2016), explored the use of Ripple Carry Adders (RCA) in Vedic architectures, highlighting their advantages in terms of reduced area and power consumption. Comparative analyses (2018) further established that while RCA offers better area and power efficiency, Carry Lookahead Adders (CLA) provide superior speed, indicating a trade-off between performance parameters.

Recent research (2020–2024) emphasizes that RCA-based Vedic multipliers are particularly suitable for small-to-medium bit- width applications and FPGA-based designs due to their simplicity and low hardware requirements. Although advanced techniques such as GDI and hybrid adder structures improve speed and power efficiency, they introduce additional design complexity.

Overall, existing literature supports RCA- based Vedic multipliers as an efficient and practical solution for low-power and resource-constrained digital systems.

III. EXISTING SYSTEM

Conventional Vedic multipliers use the Urdhva-Tiryakbhyam sutra for partial product generation, followed by accumulation using basic adders such as Half Adders and Full Adders. While accurate, this approach suffers from increased delay due to sequential carry propagation.

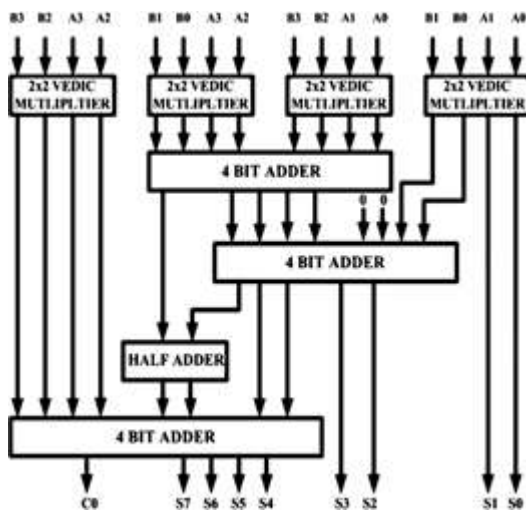


Fig.4 Block Diagram of 4-bit Vedic Multiplier

Partial products are generated using AND gates and arranged based on positional weights. These are summed using cascaded Half and Full Adders, where carries propagate through each stage, increasing delay as bit-width grows.

Advantages: Simple design, accurate results, suitable for small bit-widths. **Limitations:** High delay, increased area and power, and lack of optimization in the final addition stage.

Proposed System

To overcome the delay and resource limitations of the existing design, the proposed architecture integrates a Ripple Carry Adder (RCA) with the Urdhva-Tiryakbhyam-based multiplier. This combination improves hardware efficiency while maintaining a balance between speed, power, and area, making it suitable for FPGA and VLSI applications.

Partial products are generated using AND gates following the Urdhva-Tiryakbhyam method. These are arranged and initially reduced using basic adders, after which a Ripple Carry Adder performs the final summation. The RCA connects multiple full adders in sequence, simplifying the addition stage and reducing hardware complexity.

Advantages: Reduced hardware complexity, low power consumption, simple design, FPGA-friendly, and accurate results. **Limitations:** Linear carry propagation delay and limited scalability for large bit-width multipliers.

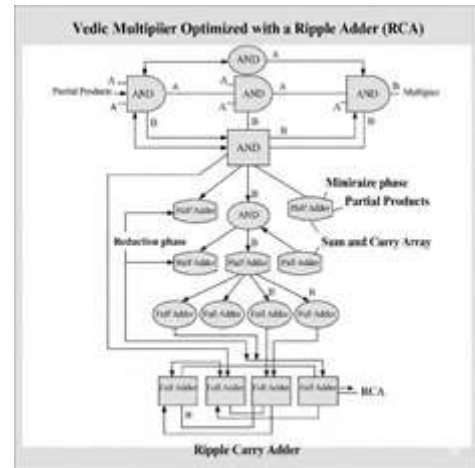


Fig 5. Block Diagram of Proposed 4 bit VEDIC Multiplier

IV. IMPLEMENTATION

The first diagram represents the internal structure of a 4-bit Vedic multiplier based on the Urdhva-Tiryakbhyam method. The inputs are divided into smaller 2-bit blocks, and partial products are generated in parallel using AND logic. These partial products are then combined using adders arranged hierarchically. The interconnections show how intermediate sums and carries are propagated through different stages to produce the final 8-bit output. This modular design improves parallelism and reduces computational delay.

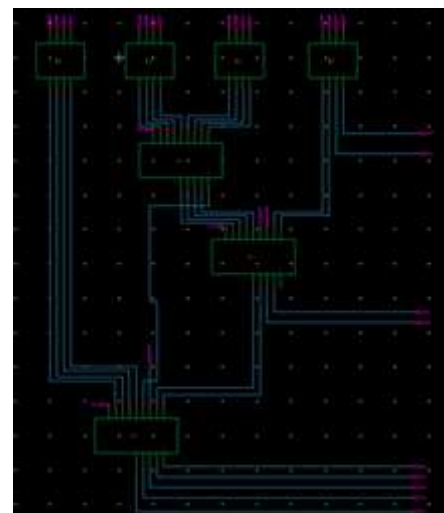


Fig 6. Schematic Diagram of 4-bit Vedic Multiplier

The second diagram illustrates the testing setup of the designed multiplier. Input signals are applied using voltage sources representing binary inputs. The multiplier block receives these inputs and produces output bits (S0–S7), which are monitored using voltage probes or measurement nodes. This setup verifies the correctness of the multiplication operation by observing output voltages corresponding to binary results. The testing environment ensures proper functionality and timing behavior of the designed circuit.

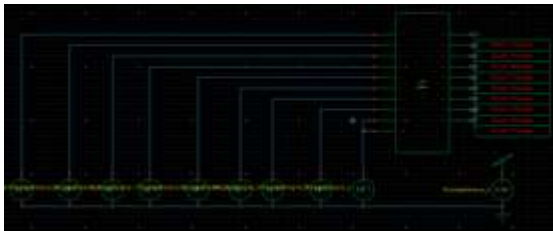


Fig.7 Schematic Diagram of 4bit Vedic Multiplier Testing

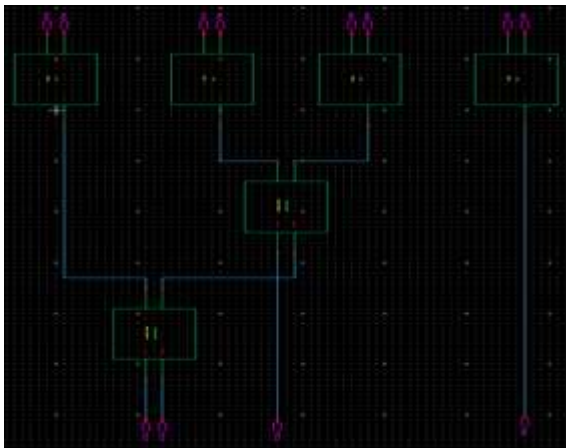


Fig 8. Schematic Diagram of 2bit Vedic Multiplier (in 4bit Vedic Multiplier)

This is a layout-style schematic showing:

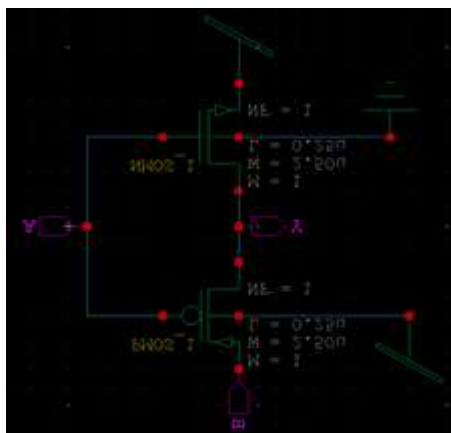


Fig 9. Schematic Diagram of OR Gate (in Full Adder)

- Multiple identical blocks (full adders)
- Interconnections for carry propagation
- Physical arrangement (likely from VLSI layout tool)

This diagram abstracts the transistor design into functional blocks:

- First block computes $A \oplus B$
- Second block combines result with
- Cin to produce Sum
- Separate logic computes Carry

The AND, OR, Half Adder, Full Adder, and Ripple Carry Adder circuits were successfully designed and verified in Tanner EDA, and then hierarchically integrated to implement 2-bit and 4-bit Vedic multipliers. Simulation waveforms obtained using W- Edit confirmed correct functionality, producing accurate outputs for test cases such as 2×2 , 3×3 , 5×7 , and 9×12 . Additionally, the Ripple Carry Adder (RCA)-based design demonstrated improved area efficiency by using fewer logic elements, along with reduced switching activity, resulting in lower power consumption and making it suitable for low-power applications.

V. CONCLUSION

The project successfully implements a Vedic multiplier using a Ripple Carry Adder in Tanner EDA. The Urdhva Tiryakbhyam Sutra enables efficient partial product generation, while the RCA simplifies addition, reducing hardware complexity. Simulation results confirm correct operation for 2-bit and 4-bit designs, with improved area and power efficiency. Overall, the design provides a good balance between simplicity, accuracy, and performance for small-to-medium digital applications.

Future Work

Future improvements include scaling to higher bit-width multipliers, replacing RCA with faster adders like Carry Lookahead Adder or Carry Save Adder, and implementing full layouts using L-Edit in Tanner EDA. Additional enhancements such as pipelining, low-power optimization techniques, and hardware implementation on FPGA/ASIC platforms can further improve performance and real-world applicability.

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