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Symmetrical DC-Sourced 11-Level Multilevel Inverter with Reduced Switching Components

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Abstract- Recent advancements in power electronics have provided a strong platform for the development of various multilevel inverter (MLI) topologies. These MLI configurations offer several notable advantages, such as high-quality staircase sinusoidal output voltage, a reduced number of power switches, and the elimination of external filters. In this paper, a symmetrical sourced base multilevel inverter topology to generate 11-level of output is proposed to minimize the number of inverter components while achieving an enhanced voltage-step generation. The proposed structure is capable of producing a high-step, staircase-type of 11-level voltage output waveform that closely approximates a sinusoidal voltage without increasing the number of power semiconductor switches. A Carrier-Based Sinusoidal Pulse Width Modulation (CB-PWM) technique is implemented at a switching frequency of 3 kHz to control the inverter operation. The simulation is carried out using MATLAB/Simulink R2019b environment. The working principle of the proposed multilevel inverter (MLI) is explained in detail. This research focuses on the design of a novel single-phase multilevel inverter with a reduced component count. The proposed MLI configuration is structured to generate the maximum possible number of voltage levels in the output AC waveform while utilizing fewer power electronic devices. Furthermore, the output characteristics of the proposed inverter are analyzed for modulation index 1 for an RL load to examine its dynamic behavior and voltage-step generation capability.

Keywords – Faculty Development Programmes, Age Differences, Professional Development, Higher Education, One-Way ANOVA, Life-Cycle Model.

I. INTRODUCTION

Multilevel inverters (MLIs) have gained significant importance in power electronic converters due to their wide range of applications and inherent advantages [1]–[3]. With the continuously increasing demand for electrical power, the integration of MLIs with modern power electronic systems has become essential [4], [5]. MLIs are extensively used in variable-frequency drives, electric vehicles, and high-voltage DC (HVDC) transmission systems [6]–[8]. In addition, they play a vital role in renewable energy conversion systems, including solar and wind energy applications [9], [10]. MLIs are particularly suitable for medium-voltage and high-power applications [11]. In MLIs, higher output voltage levels are synthesized in a staircase waveform by combining multiple DC sources [12]. This stepped output closely approximates a sinusoidal waveform, thereby reducing total harmonic distortion (THD) [13], [14]. As a result, the requirement for output filters is significantly minimized. Furthermore, the staircase nature of the output reduces the dv/dt stress across switching devices [15].

Since the voltage stress across individual switches is lower, devices with lower voltage ratings can be employed, making the system more cost-effective [16]. Many multilevel topologies also offer redundant switching states, which can be utilized to implement fault-tolerant operation [17]. The three classical MLI topologies introduced over time are the Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) configurations [18]–[20]. Although these conventional topologies provide substantial advantages over traditional two-level inverters, they suffer from certain drawbacks such as a high number of switches, multiple DC sources, and numerous capacitors [21]. To overcome these limitations, several new MLI topologies have been developed aiming to reduce component count and improve efficiency [22], [23]. These modern configurations are broadly classified into symmetrical and asymmetrical types based on the magnitude of their DC voltage sources [24].

In symmetrical MLIs, all DC sources have equal voltage levels, whereas in asymmetrical MLIs, the DC source magnitudes differ. Various modulation techniques have been proposed for MLIs, including Selective Harmonic Elimination (SHE), Space Vector Pulse Width Modulation (SVPWM), Carrier-Based Pulse Width Modulation (CB-PWM), and Nearest Level Control (NLC) [13], [25]. Several studies also discuss the use of H-bridge configurations to generate positive and negative voltage polarities [20]. Moreover, some reported topologies require a greater number of DC sources than power switches, which increases system complexity [23]. In this paper, a symmetrical 11-level MLI is proposed. The performance of the proposed topology is evaluated using MATLAB/Simulink simulations for RL-load in different modulation index. The remainder of the paper is organized as follows: Section 3 describes the operating modes and modulation technique of the proposed inverter; Section 4 presents the modes of operation; and Section 5 discusses the simulation parameters and obtained results.

II. PROPOSED CIRCUIT TOPOLOGY

The proposed 11-level MLI is depicted in the Fig.1. The topology is fundamentally divided into two distinct functional blocks: the level generation unit and the polarity generation unit. The proposed topology utilizes a total of ten power switches. These are categorized based on their switching characteristics: Bidirectional Switches: T8, T9, and T10. These are crucial for facilitating bidirectional current flow, which allows for flexible voltage level synthesis and proper operation across all four quadrants. Unidirectional Switches: The remaining switches (T1 through T7) operate in a standard unidirectional configuration. The inverter is configured in a symmetric mode, meaning all five DC five voltage sources possess equal magnitude. This symmetric arrangement offers significant advantages, including balanced voltage stress across the switching devices and a more streamlined modulation and control strategy. Level Generation Unit synthesizes the stepped DC voltage profile. By selectively activating specific switches, the circuit connects or bypasses the five equal DC sources in various series combinations to generate the desired intermediate voltage levels. Polarity Generation Unit: comprised of four switches acts as a full-bridge inverter. It effectively maps the synthesized stepped DC voltage to both positive and negative half-cycles of the output waveform. This allows the inverter to produce a complete AC output without requiring additional DC power sources.

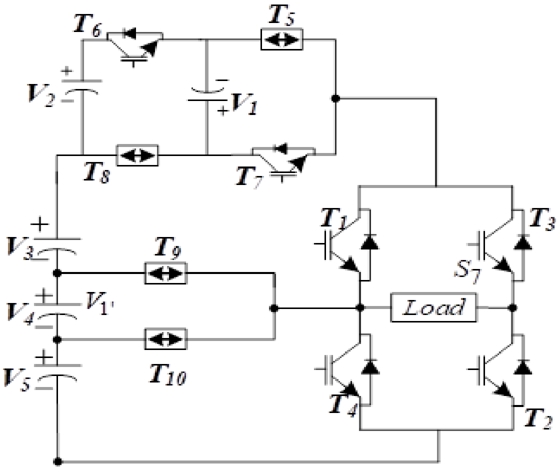


Fig. 1. Proposed 11-level MLI topology

III. MODULATION AND CONTROL OF MLI

In Fig. 2(a), multiple high-frequency triangular carrier signals are compared with a low-frequency sinusoidal reference signal. The reference waveform determines the fundamental output frequency, while the carrier signals operate at a higher switching frequency (3 kHz). The intersection points between the sinusoidal reference and the carrier signals generate the gating pulses required for switching the power semiconductor devices. The amplitude of the reference signal controls the modulation index, which directly influences the output voltage magnitude. Fig. 2(b) presents the corresponding stepped output voltage waveform obtained from the switching process. As the reference sine wave crosses different carrier bands, the inverter switches between various voltage levels, producing a staircase waveform. This stepped waveform closely approximates a sinusoidal output, thereby reducing total harmonic distortion (THD). The increased number of voltage levels improves waveform quality and minimizes dv/dt stress across the switches.

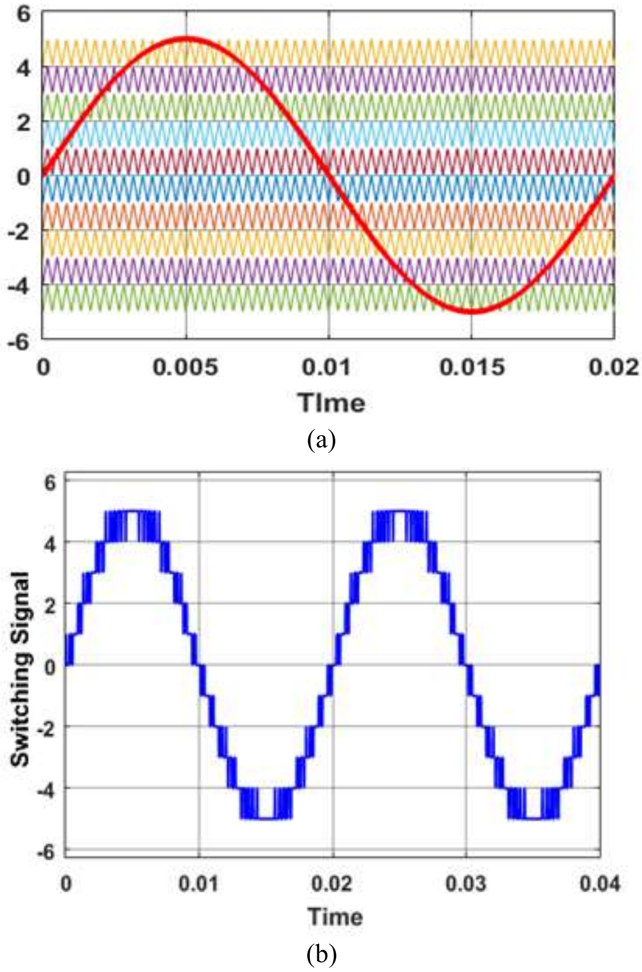


Fig. 2: PWM signal generation: (a) Comparison between multiple carrier waves and the reference signal; (b) Resulting switching signal for the 11-level MLI.

IV. MODES OF OPERATION

The various voltage levels of the proposed 11-level inverter are produced by selecting appropriate combinations of switches, as summarized in Table 1. Each output level is generated by turning ON specific switches (indicated by √) while keeping the remaining switches OFF (indicated by ×). For the maximum positive level, +5Vdc, switches S1, S2, S6, and S7 are ON. The +4Vdc level is obtained by activating S1, S2, S5, and S6, while +3Vdc is produced using S1, S2, S7, and S8. The +2Vdc and +1Vdc levels are achieved by turning ON S2 with S9 and S2 with S10, respectively. The zero-voltage level (0Vdc) is generated by switching ON S2 and S4. For the negative voltage levels, −1Vdc is obtained with S3, S7, S8, and S9 ON; −2Vdc with S3, S7, S8, and S10; −3Vdc with S3, S4, S7, and S8; −4Vdc with S3, S4, S5, and S6; and −5Vdc with S3, S4, S6, and S7. Thus, each of the eleven voltage levels is realized through a unique switching combination, ensuring proper connection of the DC sources to synthesize the desired stepped output waveform. The different modes of voltage generation for the 11-level inverter are illustrated in Fig. 3. The positive half-cycle voltage generation path of the proposed topology is represented by the green arrow while the negative half-cycle is represented by the red one.

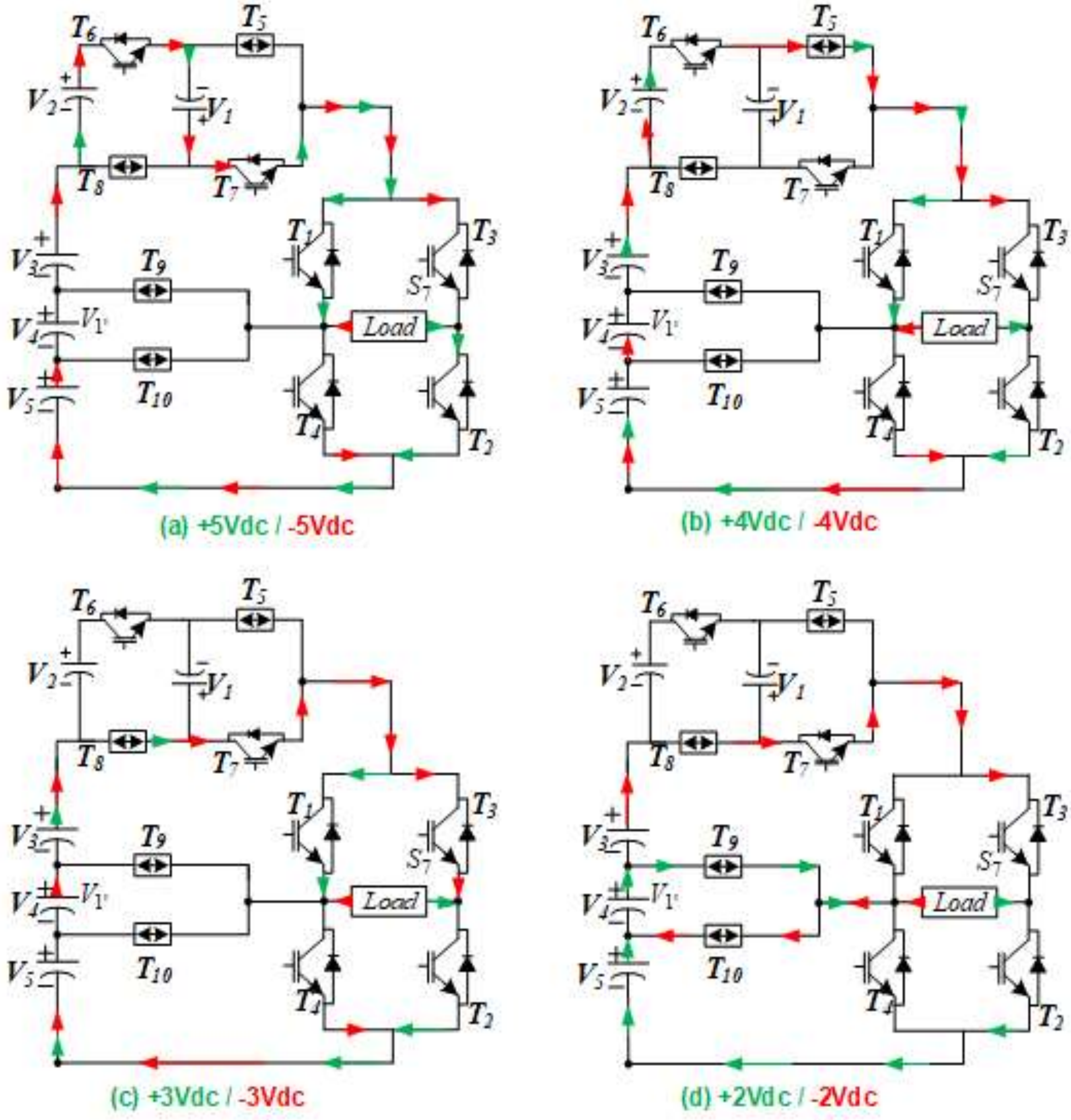
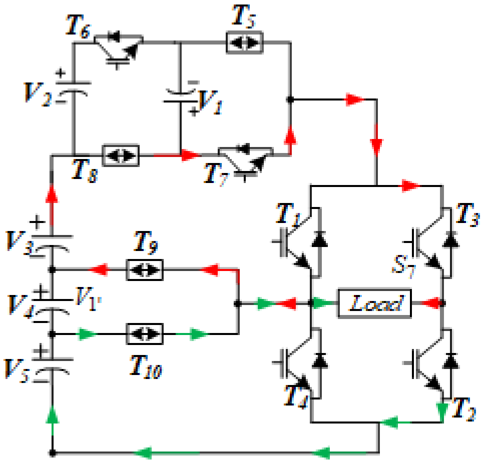
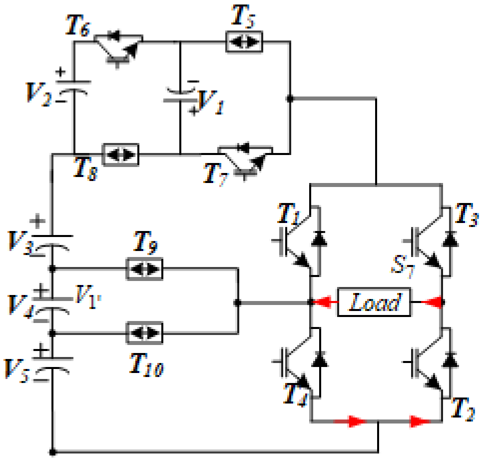


Fig.3. Modes of operation for positive and negative half cycle of the proposed 11-level MLI



(e) +1Vdc / -1Vdc



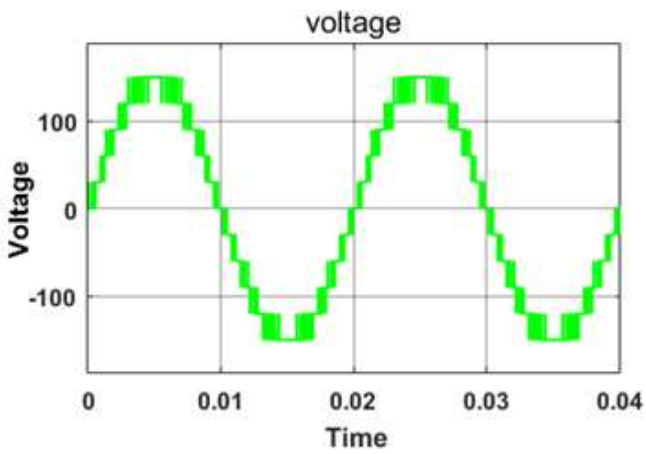
(f) 0 Vdc

Table. 1. Switching status of switches for 11-level MLI

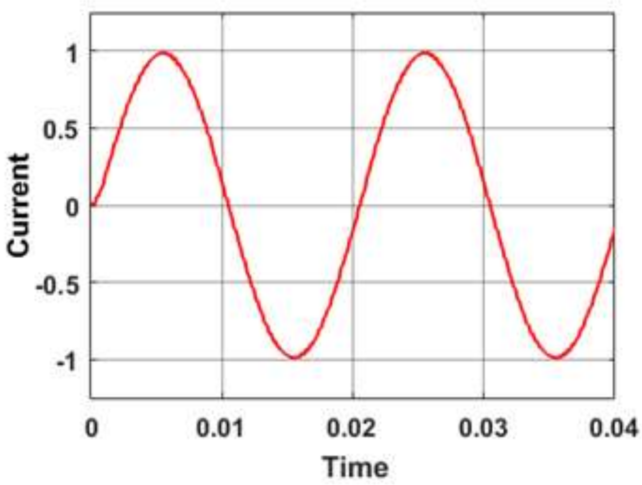
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}
$+5V_{dc}$	✓	✓	x	x	x	✓	✓	x	x	x
$+4V_{dc}$	✓	✓	x	x	✓	✓	x	x	x	x
$+3V_{dc}$	✓	✓	x	x	x	x	✓	✓	x	x
$+2V_{dc}$	x	✓	x	x	x	x	x	x	✓	x
$+1V_{dc}$	x	✓	x	x	x	x	x	x	x	✓
$0V_{dc}$	x	✓	x	✓	x	x	x	x	x	x
$-1V_{dc}$	x	x	✓	x	x	x	✓	✓	✓	x
$-2V_{dc}$	x	x	✓	x	x	x	✓	✓	x	✓
$-3V_{dc}$	x	x	✓	✓	x	x	✓	✓	x	x
$-4V_{dc}$	x	x	✓	✓	✓	✓	x	x	x	x
$-5V_{dc}$	x	x	✓	✓		✓	✓	x	x	x

V. SIMULATION AND EXPERIMENTAL RESULTS

This section presents the simulation study of the proposed 11-level MLI. The system is modeled and analyzed using MATLAB and Simulink to evaluate its performance under specified operating conditions. The selected DC source magnitudes are V1= V2 = V3 = V4 = V5 = 30 V. This equal configuration enables symmetrical operation and facilitates the generation of 11 output voltage levels. The inverter performance is examined at modulation indices of 1 with an RL load having R = 150 ohm and L = 75 mH. Under these conditions, the maximum output voltage reaches 150 V, and the corresponding peak load current is 1 A as depicted in the Fig. 4.(a) and Fig. 4(b) respectively.



(a)



(b)

Fig. 4. Simulation results for the (a) output voltage; (b) load current; at MI = 1

VI. CONCLUSION

This paper presented a symmetrical 11-level multilevel inverter (MLI) topology with a reduced number of power switches and a simple structural design. The proposed configuration consists of ten switches, including three bidirectional switches, and is divided into a level generation unit and a polarity generation (full-bridge) unit. The symmetric arrangement of five equal 30 V DC sources ensures balanced voltage stress across the devices and simplifies the modulation strategy. By selectively connecting or bypassing the DC sources, the inverter successfully generates eleven distinct voltage levels, producing an improved stepped output waveform. The polarity generation unit enables the production of both positive and negative half-cycles without requiring additional DC sources. The proposed topology was modeled and simulated in the MATLAB/Simulink environment under RL load conditions (150 Ω, 75 mH) at a modulation index of 1. The results confirm satisfactory performance, achieving a maximum output voltage of 150 V and a peak load current of 1 A. Overall, the developed 11-level MLI demonstrates effective voltage level synthesis, balanced operation, and practical suitability for medium-voltage and renewable energy applications.

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