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Design of low power high speed comparators for flash ADC applications

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Abstract- The fundamental requirements of VLSI design are high speed, low power and compact size. Comparators are basic building elements for designing of ADCs. In this work, a dynamic comparator is proposed which is based on double tail architecture. A modification in the form of an extra transistor (control transistor Msc) has been added to the previous circuit [10] along with a reduction in the length of the MOSFET transistor from 180-nm to 90-nm. The proposed comparator attains a sampling speed of 3.3 GHz at a supply voltage of 1.2V and is designed on 90nm CMOS Technology. The power consumption in terms of energy per conversion is 0.2221198 pico Joule and the worst case delay (for ΔV of 1 mV) is found to be 17.7 pico seconds. Apart from the supply voltage, the proposed comparator attains better output parameters compared to previously existing work.

Keywords- Analog to Digital Converter (ADC), Comparator, Double Clocked Comparator, Sampling Frequency, Power Consumption, Worst case delay, Technology Size.

I. INTRODUCTION

Comparator is basic building block for designing of high speed analog to digital converters (ADCs) like flash ADCs. Analog to digital converters (ADCs) require high speed, low power consumption with small chip area. The designing of a comparator can begin with power consumption operation speed and their gains are constrained. The dynamic regenerative comparators are preferred for design of high speed low power ADCs, this is due to the positive feedback strengthen the signal strength in this converter [1]-[3]. The comparator si also termed as a one bit analog to digital converter where in the comparison is done between two signals and an output in terms of 0 or 1 is generated by the circuit.

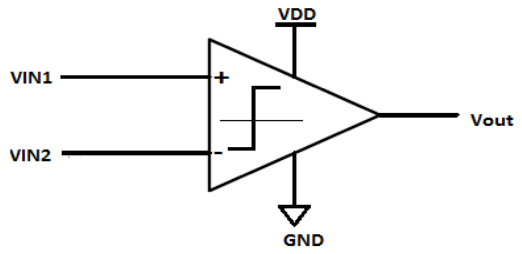

Fig.1 The basic block diagram of a comparator

Mathematically,

If V_in1>V_in2,V_o=V_DD (1)

Else If V_IN1<V_in2,V_O=gnd (2)

Here,

V_DD is considered as logic 1 gnd is considered as logic 0.

Often, logic 1 is termed as V_(OH) i.e. High Output Voltage and gnd is termed as V_(OL) i.e. Low Output Voltage.The comparator is comprised on some stages of operation. A stages of a regenerative comparator are shown in fig.2, the basic blocks of a high performance regenerative comparator consist (1) pre-amplification stage, (2) Regenerative latch Stage or positive feedback stage and (3) post-amplification stage or output buffer stage. The input preamplifier stage takes the inputs and amplifies the signals to improve signal sensitivity and feed to input of Regenerative latch or positive feedback stage (i.e amplifies minimum input signal with which the comparator can make a decision). It also isolates the input of the comparator from kickback noise produced during positive feedback stage in the regenerative comparator [4]-[5]. The decision stage takes amplified input from the preamplifier stage and it determines which of the input signals is large.

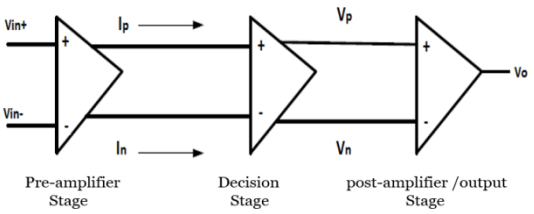

Fig.2 Stages of Regerative Comparator

The preamplifier circuit stage is a differential amplifier and the sizes of its transistors determine the input capacitance and differential amplifier transconductance gm. The relationship between input voltage and output current Ip and Inis given by

Ip=gm/2(Vin+ -Vin-) +Is/2 = Is-In(3)

Where,

Ip=-In

The decision stage is very important stage in the comparator and it must be capable to make decision up to mV-level signals. The circuit uses positive feedback to strengthen the signal level to improve the comparator sensitivity [1]. The final stage of the comparator is output buffer or post-amplifier, the main role of this stage is to covert the output of decision circuit into a logic signal (i.e. logic '0' (0V) or logic '1' (VDD) [6].

II.CONVENTIONAL DOUBLE TAIL COMPARATOR

A conventional dynamic double-tail comparator is shown in fig.3.This comparator can operate at lower power supply voltages because this topology has less stacking compared to the conventional dynamic comparator. A large current in the latching stage is drawn due to double tails [7].

The working of this comparator can be understood by transition of clock pulse from reset phase or CLK = 0 to CLK=1.During reset phase or CLK= 0, both tail transistorsMtail1, and Mtail2 are in cut off and the transistors M3-M4turn on.M3-M4 pull up fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 start conducting and these transistors discharge or pull down the output nodes to ground.

During decision-making phase when CLK =VDD, the tail transistors Mtail1 andMtail2 are on and they start conducting, and the transistors M3-M4turn off, the voltages at nodes fn and fp drop with the rate defined by Itail1/Cfn(p) and an input-dependent differential a voltage ΔVf will build up at input of MR1 and MR2which is independent of differential inputs. The intermediate transistors stage MR1 and MR2 will pass ΔVf to the decision circuit and it also provides a good isolation between input and output, which reduces the kickback noise during positive feedback [4].The delay of this comparator depends on two main parts, the capacitive charging of the loadcapacitancet0 and the latch regeneration time tlatch.The total delay of this comparator is achieved as follows

tdelay = to + tlatch (4)

T_DELAY= 2(Vtn CL)/IB1 + CL/(gm,eff)ln((VDD/2)/ΔVo) (5)

From the previous work on double tail comparator, some important notes can be concluded.

It has been observed from previous work that at the beginning of the reset phase, the 'outp' and 'outn' need to coincide at the same starting voltage point at the outset of the Decision Making Phase. Since during every voltage comparison, voltages 'outp' and 'outn' start together and diverge depending upon the stronger value among the two.

III. DOUBLE TAIL COMPARATOR

In this work , an extra transistor (control transistor Msc) is added to double tail comparator to improve the double tail comparator performance in terms of frequency and energy per conversion. The shorting transistor brings down the voltage swing of the output from VDD to VDD/2. The length of the MOSFET transistor is reduced from 180-nm (previous work done [10]) to 90-nm. Reduction in channel length reduces the MOS capacitance hence reduces the MOS charging and discharging time. This reduces the delay and increases the frequency. The technology size and voltage swing of output are related to the energy per conversion, delay and speed of the comparator.

When Clk=0,

1. Mtail1 and Mtail2 = 'off '

M3 and M4 = 'on'

2. fp and fn charge to VDD , then

MR1 and MR2 = 'on' pull outn and outp to the ground

3. Therefore voltage at outn and outp = 'zero' . Comparator is not working. So, at low logic level of clock, circuit is disconnected from supply.

However, when Clk=1,

1. Mtail1 and Mtail2 = 'ON '

M3 and M4 = 'off' and M1 and M2 = 'ON' fp and fn discharge to 'ground' with different rate according to input voltages (INN and INP). This is because fp and fn discharge to gnd through M1 and M2 (both NMOS). If Inn>Inp, this means more positive gate voltage goes to M1 thereby increasing the current of M1. This makes M1, hence fp discharge to gnd faster than fn.

2. Let INN > INP then fp drop drops faster than fn MR1 turns off faster than MR2, discharges towards gnd and isolates from outn. Now outn start charging to VDD (logic 1) through the path M7 to VDD. Since, outn is connected to M8 (PMOS) and M10 (NMOS), therefore, M8 turns off (logic 1 at gate). Now, outp is disconnected from VDD since M8 is off but outp is connected to gnd since M10 (NMOS) is ON. So outp goes to gnd (logic 0) while outn remains at VDD (logic 1)

3. When Clk changes from '1' to '0' (INN > INP), clk-bar goes to 1. Control transistor Msc starts conducting (NMOS) and shorts the output nodes outp and outn and both nodes are at VDD/2 (common potential). The previous comparison was already over after outn was 1 and outp was 0. Now, outn and outp are at same potential before the next comparison starts (when clock will again go from 0 to 1).

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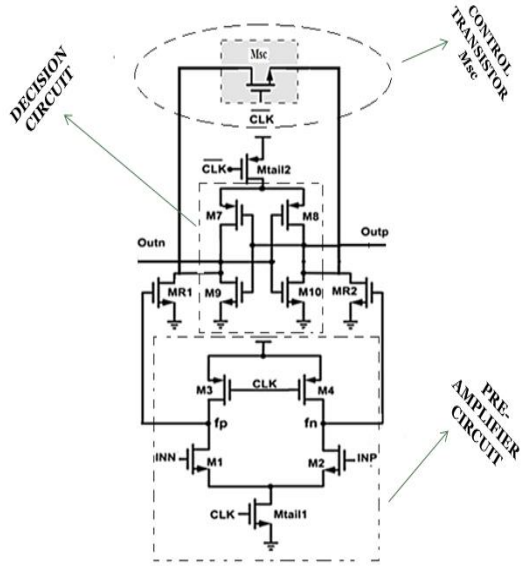

Fig.3 Circuit of Proposed Comparator.

Out p and Out n remain at the same potential by invoking the voltage divider rule. The modelling for the starting point of the output at the beginning of each conversion is given below using the voltage divider.

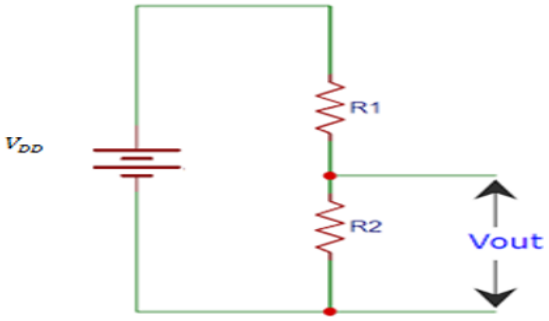

Fig.4. The Voltage Divider Circuit.

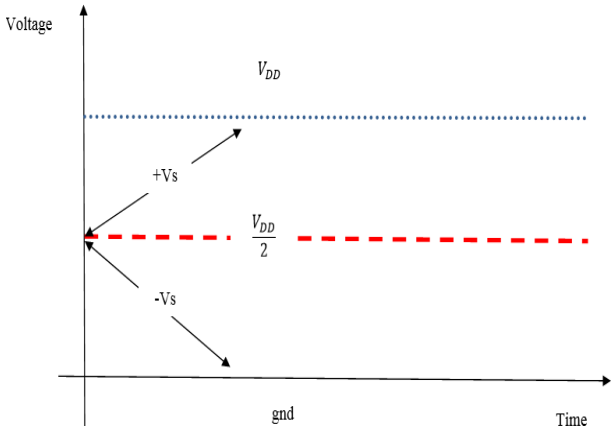

Fig.5. Voltage Swing of Output with proposed approach.

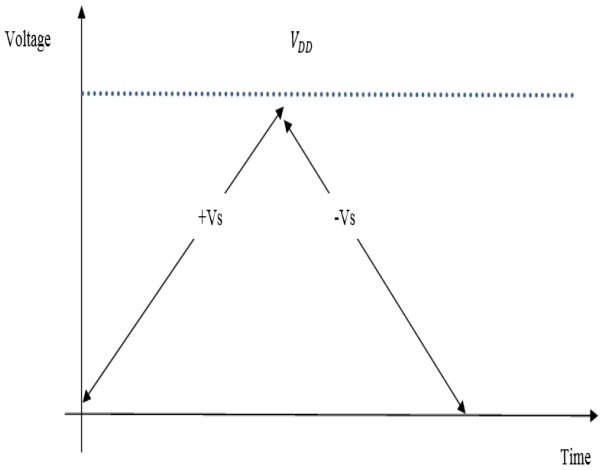

Fig.6. Voltage Swing with Conventional Approach.

Here,
V_DD represents supply voltage
gnd represents ground
Vs represents voltage swing
It can be clearly seen that the voltage swing reduces form Vdd to Vdd/2 thereby considerably reducing the time the output voltage needs to travel before each conversion.
The output voltage across R2 is given by
⟦ V⟧_out=R2/(R1+R2) V_DD (6)
If the terminals Outp and Outn (one of which is at V_DDand the other is at gnd), are shorted, then assuming the bulk resistance of the shorting transistor to be acting equally at both terminals, the output voltage boils down to:
V_out=R/(R+R) V_DD=V_DD/2 (7)
Thus in the beginning of every conversion, the outputs start atV_DD/2 in place of V_DD
But this phenomenon of pulling up and pulling down doesn't need both the transistors to reach a common Zero Voltage Level rather it begins the reset state as soon as both transistors reach a Common Voltage Level. even seen from Fig.4.3 that it takes lesser time for both the transistors to reach a common voltage level as they don't need to traverse the Entire Dynamic Range between the high and low voltage levels. This effect considerably reduces the sampling time thereby bringing about a substantial change in the Maximum Sampling Frequency. It holds common ground of V_DD/2. Thus, clearly the comparators output reaches to V_DDor 0 V depending upon the position of the output voltages.

IV.RESULTS

The proposed dynamic double clocked comparator is simulated with the help of Cadence and observed the output of comparator. CMOS Technology and W/L Ratio: The technology used here is 90nm which is considerably less compared to the common earlier technology scale of 180nm. The value of ß, i.e. W/L is 4:3. The results obtained from the model of the proposed comparator can be summarized and explained under the following heads

individually, for which the table tabulating the final results has been referred: The evaluation parameters are:

1. Maximum sampling frequency
2. Power consumption or energy per conversion
3. Supply Voltage
4. Worst Case delay
5. Technology size

The simulation can be performed on any of the commonly used standard EDA tools such as Microwind, EDA Tanner or Cadence. Similar results are obtained on Microwind, EDA Tanner and Cadence. The simulations furnished here are for the Cadence Virtuoso tool.

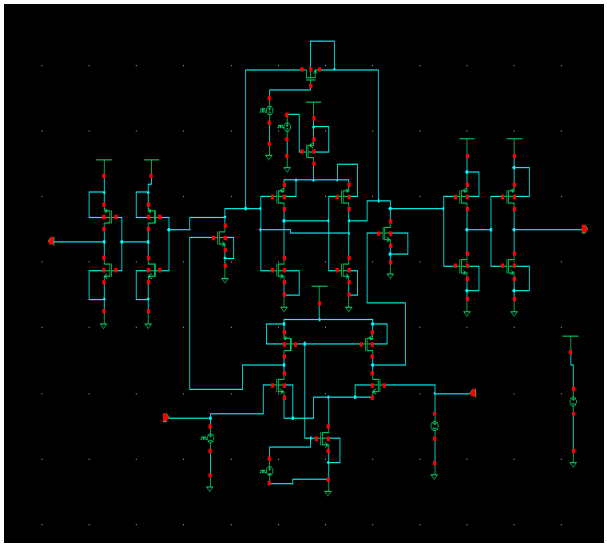

Fig.7. Proposed Double tail Comparator circuit design in Cadence.

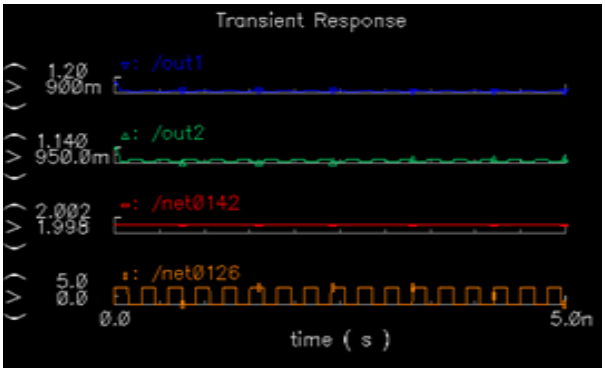

Fig.8. Output of Proposed Double tail Comparator circuit at clock frequency 3.3 GHz.

It can be clearly seen that the voltage swing reduces form Vdd to Vdd/2 thereby considerably reducing the time the output voltage needs to travel before each conversion.

Clock pulse time period = 0.325ns

The clock frequency of the proposed comparator can be calculated by the given relation

Maximum clock frequency = 1/(Clock pulse time period)Hz (6)

Maximum sampling frequency = 1/(0.3 x ⟦10⟧^(-9))Hz (7)

Maximum sampling frequency ≈ 3.33x109 Hz

Another important parameter which is critical for the comparator design is the power consumption. It should however noted that the absolute power consumption in this case is immaterial. The reason being the fact that if the comparator circuit works for a longer time, then the overall power consumption will increase.

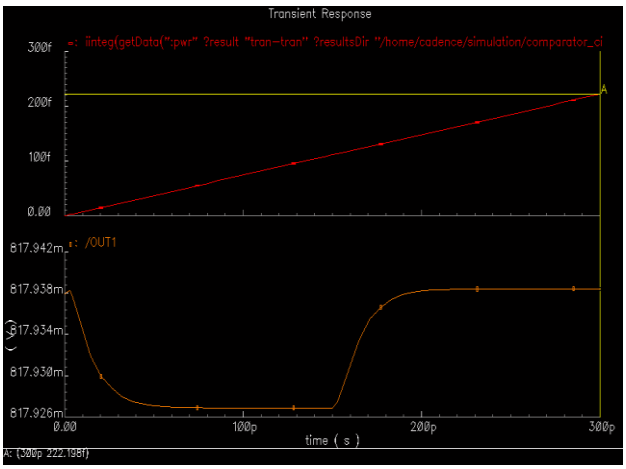

Fig.9. Transient output for Energy per Conversion.

Mathematically,

P_TOT=f(t) (8)

Here,

P_TOT is the total power consumption

f represents a function of

t represents time

Hence, the apt way to measure the power consumption of a comparator circuit is by measuring the power for one clock cycle i.e. energy per consumption. This can be computed by computing the area under curve of Power-time curve. Mathematically, energy per conversion is given by:

E_pc=∫_0^T▒p(t)dt (9)

Here,

E_pc is the energy per conversion

p(t) is the power as a function of time

t is the time metric

From the figure, it can be seen that the energy per conversion for one clock cycle i.e. 0.3ns or 300 fs is 222.198 fJ i.e. 0.222198pJ.

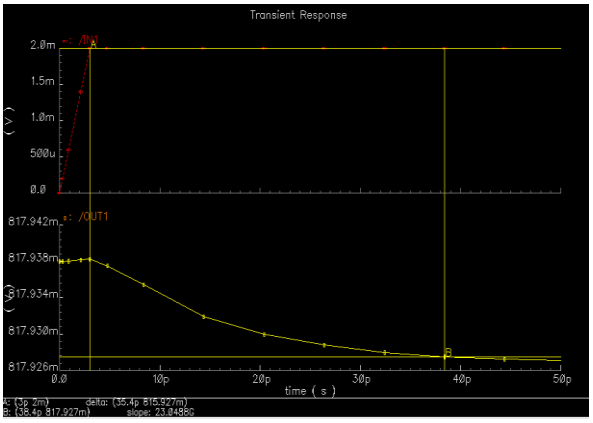

Fig.10.Output Delay.

The delay in the output again depends on the voltage swing magnitude. For example, the output delay would increase if the output has to rise or fall to a larger magnitude as compared to a smaller magnitude. Hence the worst case delay is computed for a voltage swing of :

⟦ΔV⟧_in=1mV (10)

It can be clearly seen from figure 4.5 that the delay from the transition of output 1 from high to a point where it attains steady state is:

Delay_TOT=35.4ps (11)

The voltage swing is:

ΔV=817.927-815.927=2mV (12)

Thus the worst case delay for ΔV=1mV is:Delay (ΔV=ImV)=35.4/2=17.7ps

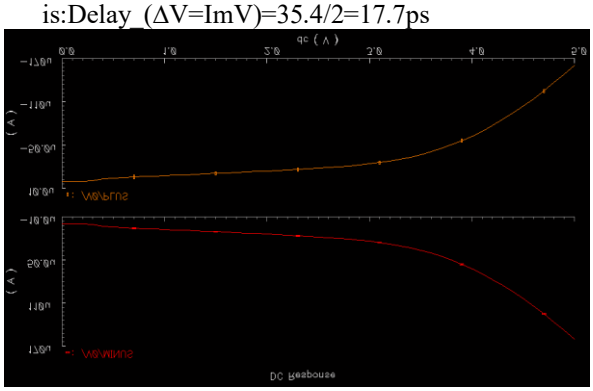

Fig.11. DC Analysis of Proposed Comparator.

The figure above depicts the DC response of the proposed comparator. It can be seen that the dc voltage consumes time to reach the dc steady state voltage.

V.CONCLUSION

It can be concluded from the previous discussions that the comparator design has been implemented on 90nm CMOS technology on Cadence adhering to the state of the art standards laid down for VLSI design. The comparator designed here uses a shorting or switching transistor that reduces the dynamic range of the voltage swing from the entire value of supply voltage VDD to half of it thereby minimizing the delay of the comparator. The proposed comparator attains a sampling speed of 3.3 GHz at a supply voltage of 1.2V and is designed on 90nm. The power conversion in terms of energy per conversion is 0.2221198 pico Joule and the worst case delay (for ΔV of 1 mV) is found to be 17.7 pico seconds. Apart from the supply voltage, the proposed comparator attains better design parameters compared to previously existing work [10].

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