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Design of Low Power SRAM using Power Gating and DG-MOS Technology

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Abstract- The paper presents a 6T SRAM based on DG-MOSFET and Sleep Transistor for leakage current reduction. A bulk 6T SRAM is implemented and simulated for the proper functioning of the SRAM cell for 1 bit storage on the 90nm technology. We have used a DG-MOSFET for reducing the threshold voltage and so the power consumption. On the circuit level, the static power dissipation has been considered. Reduction of leakage current is done by using Sleep Transistor technique. The DG-MOSFET based 6T SRAM with Sleep Transistor technique is implemented and simulated. The designing and simulation tool we used is Cadence virtuoso. The transient, DC and parametric analysis provide the results. The transient response helps demonstrate the proper functioning of the SRAM, while the DC response provides results related to voltage values, which are useful for understanding the power consumption of the circuit. The parametric analysis gives different values of leakage current on different width of the MOSFET which shows that the bulk 6T SRAM consumes more power than DG-MOSFET based 6T SRAM with Sleep Transistor. The results indicate improved performance of the proposed static RAM compared to the conventional static RAM in terms of leakage reduction.

Keywords: Static RAM, Leakage Current, Bulk 6T SRAM, DG-MOSFET, Sleep Transistor.

I. INTRODUCTION

Recent memory technologies including SRAM, DRAM and flash memory are facing technology limits to their continued upgrading. Accumulation of new materials to improve gate SiO_2oxide concert and consistency can only add to circuit costs [1]. This fact has led to intense efforts to ripen new memory technologies. This type of memory being addressed includes primary and secondary memory, which are volatile.

However, the BIOS battery helps provide them with power supply to maintain their hold mode [2]-[13].. Most of these new technologies are less affected by short channel effect on memories and can be used for long term storage or to provide a memory that does not lose information automatically. DG-MOSFET based SRAM cells will begin a new substitute to CMOS based SRAM and DRAM cells in a next few years.

The rate of development of compact memories more and more with fewer amounts of its drawbacks helps to replace CMOS technologies to DG-MOSFET based emerging technologies. Moving to a DG-MOSFET based disk and cache devices will reduce power usage and dissipation directly as well as with new power saving modes, and it provides the better performance in lesser channel length. The use of double gate technology as embedded memory with CMOS logic has numerous applications in the electronics industry. [4]-[6].

1.Implementation And Design 6t Sram Cell

As SRAM cell is the most traditional circuit in system on chip (SoC) technology which scales down size of cell and also voltage [7]-[8]. 6T SRAM cell have total of six transistors in which four are NMOS and two are PMOS. Out of six, four transistors can be seen to form a back to back combination of complementary MOS inverter pairs which hold the bit, while other two NMOS transistors work to pass bit line data in bi-stable latched that shown in Figure 1. Thus the basic CMOS inverter cell comprises of (N1, N2, P1, P2) while N3 and N4 act as the pass transistors governed by the bit line (BL and BLB)

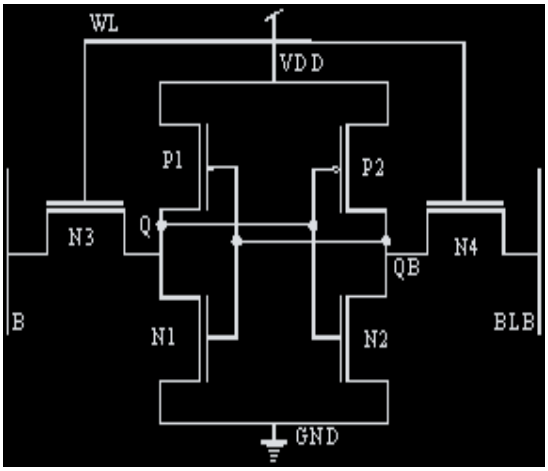

Figure 1 Conventional 6T SRAM Cell

In 6T SRAM Cell there are two bit lines BL and BLB which are complement of each other but of same period and Q and QB are also complemented outputs and a single word line WL. There are three modes of operation in SRAM cell i.e. Hold mode, active mode, stand-by mode. In stand-by mode WL goes high to low (WL=0) and the bit line either 0 or 1, it just holds the data inside the cross coupled inverters. In write mode, word line goes low to high (WL=1) and new data is put into BL bit line, that data writes on Q and QB outputs using pass transistors. When word line goes high to low (WL=0) and the data on bit line (BL) is pre-charged or left floating, the value stored during write operation at output Q goes through pass transistor to one of bit line that is discharging and another one line is pre-charging and this charging and discharging of data is sensed by sense amplifier during read operation and amplifies the data which is used further at outputs Q and QB [9].

II.PROPOSED DG-MOSFET BASED SRAM CELL

The memory design is very simple just to hold single bit data. The memory that we are using in our application purpose is the 1-bit of memory due to that data retention and power dissipation in are major issues, so future requires technology which has scaling capability itself to reduce size because of that DG--MOSFET becomes point of line for this issue. For better reduction in short channel effects, power supply scaling capability, and low power dissipation, the DG-MOSFET is a superior choice compared to conventional CMOS. The MuGFET often used as a CMOS variant used in memory chips in general perform better in terms of leakage and scalability with improved fan out. The low power design is suitable through DG-MOSFET due to no body biasing for leakage reduction and it works on less power supply voltage compare to CMOS logic. DG-MOSFET width needed efforts to design SRAM cell by adjusting V_{th} of SRAM cell. Hence, the design of the static RAM for different V_{th} values needs to be analyzed.

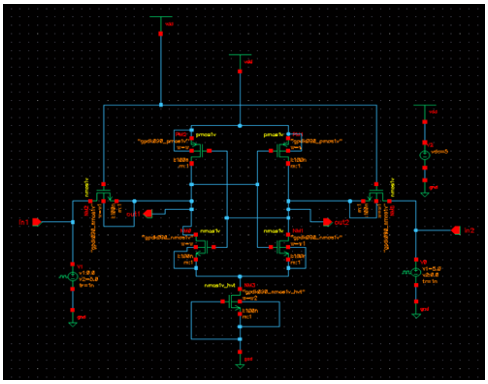

Figure 2 DG-MOSFET based 6T SRAM Cell

Leakage current The steady state operation of CMOS technology, in general doesn't exhibit power dissipation under static operational mode [10]-[11]. In practical situations though, degraded levels of voltage are fed to gate comprising of CMOS transistors and a subsequent flow of current can be seen from power supply to ground, which is often termed as static biasing current. In Fig. 4, depicts the situation in which an inverter is driven by a pass transistor [12]. On analyzing the circuit, we reach to the result that voltage at node A is degraded (Vdd-Vth). The inverter input being high (Vdd-Vth), the output would be low. Since the PMOS generally allows for a weak current , the flow from the Vdd terminal to the ground, it results in a low magnitude of leakage current. Thus static biasing current come into the picture due to the aforesaid conditions. Static currents which flow from Vdd to ground, without degrading the inputs is known as leakage power. With the advent of technology resulting in scaling, supply voltage must be reduced to address dynamic power and issues pertaining to reliability [13]. This in turn needs a modification in the device fabrication which would maneuver the threshold voltage for device operation and would have a cascading effect on the sub-threshold value of the current of the device to increase exponentially [14].

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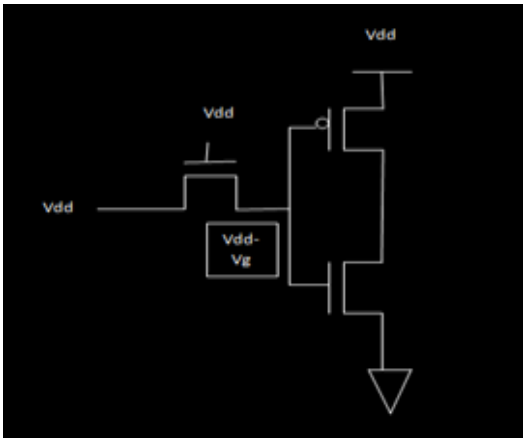

Figure.3 Degraded voltage level at the input node of a CMOS inverter results in static biasing power consumption.

During the condition Vgs<Vth, the NMOS is off-state. Still, an unwanted value of leakage current might flow from the drain terminal to the source terminal [15]. The currents flowing below the actual threshold voltage for the MOSFET is termed as the sub-threshold current. It is observed under the conditions of no gate voltage and supply voltage applied. It becomes mandatory for Ioff to have a very small value so that the circuit consumes negligible static power (typically in stand by mode) [16].

As an illustration, let us consider Ioff be 100nA per transistor, a simple cell-phone chip that contains 100,000,000 transistors would consume almost a standby

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current (10A) that would result in the battery draining out briskly even without the cell phone getting any call. A desk-top computer may still be used but at the cost consuming power from the a.c. mains supply or UPS and moreover causing excessive heating problems. When Vgs is below Vth, Ids behaves as an exponential function of Vgs [17]. When Vgs is below Vth, the concentration of inversion electron (ns) in general flow in the sub-threshold applied voltage range when the threshold is not reached. This causes a leakage current to flow which can be computed using the equivalent circuit of the CMOS inverter as [18]-[20]:

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{oxe}}{C_{oxe}+C_{dep}} \equiv \frac{1}{\eta} \quad (1)$$

$$\eta = 1 + \frac{C_{dep}}{C_{oxe}} \quad (2)$$

Integrating Eq. (1) yields

$$\varphi_s = constant + \frac{V_g}{\eta} \quad (3)$$

Ids is proportional to n_s, therefore, we obtain:

$$I_{ds} \propto n_s \propto e^{\frac{q\varphi_s}{kT}} \quad (4)$$

$$I_{ds} \propto e^{q(constant+\frac{V_g}{\eta})} \propto e^{\frac{qV_g}{\eta kT}} \quad (5)$$

Eqn.5 on substituting standard values boils down to:

$$I_{ds}(\text{nA}) = 100 . \frac{W}{L} . e^{\frac{q(V_{gs}-V_{th})}{\eta kT}} \quad (6)$$

Considering the fact that the fuction exp(qVgs/kT) changes by a factor of 10 for every 60 mV change in Vgs, hence exp(qVgs/ hkT) changes by a factor of 10 for every h×60mV. As an illustration, if h=1.5, then Ids drops by 10 times for every 90mV of decrease in Vgs below Vt. It should be noted that h×60mV is called the subthreshold swing and represented by the symbol, S.

$$S = \eta . 60 \text{ mV} . \frac{T}{300} \quad (7)$$

Experimental results also show that a parametric sweeping of 300mV affects the leakage current value in the magnitude of pA. The swing is expressed as:

$$S = \eta . 60 \text{ mV} . \frac{T}{300} \quad (7)$$

$$I_{ds}(\text{nA}) = 10\frac{W}{L} e^{\frac{q(V_{gs}-V_{th})}{\eta kT}} \quad (8)$$

$$I_{off}(\text{nA}) = 100\frac{W}{L} 10^{\frac{-V_{th}}{S}} \quad (9)$$

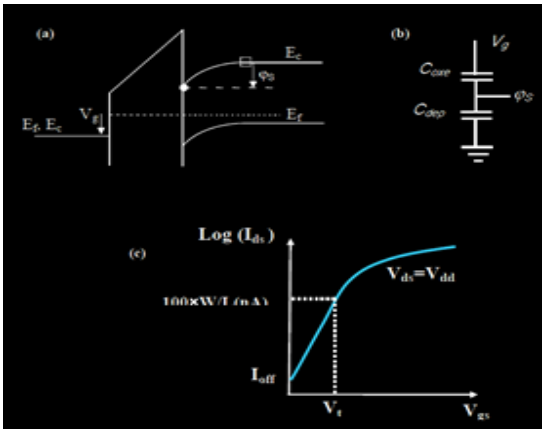

Figure. 4 (a) When Vg is increased, Ec at the surface is pulled closer to Ef, causing ns and Ids to rise; (b) equivalent capacitance network; (c) Subthreshold IV with Vt and Ioff

Ioff depicted in Fig. 5 (c) results in leakage for ultra low power (UPL) systems. To reduce the power consumption in the ULP devices, threshold voltages should be maintained near the sub-threshold mark called as the near-threshold regime. One is choosing a large value of Vth, but this is not an optimal solution since it would reduce Ion and hence increase the gate delays. The other more feasible solution is to reduce the subthreshold swingn (S). Another way to reduce S is to reduce Ioff, so that the transistors operate at a lower temperature. The last mentioned technique is seldom used for the additional cost that cooling needs [21].

III.SIMULATION AND RESULTS

The simulation can be tested on the following EDA tools:

- Cadence Virtuoso
- EDA Tanner
- Microwind.

The designed statc RAM circuit has been implemented on Cadence Virtuoso tool on the 90nm CMOS technology.

We represent the simulation waveform of the three types of analysis:

1. Transient Analysis of the input and output circuits.
2. DC Analysis of the DC voltage source.
3. Leakage current Analysis

Primarily, two circuit configurations are considered and analyzed which are the bulk 6T SRAM and the DGMOSFET based 6T SRAM cell with sleep transistor (employing power gating). By doing all the above analysis and comparison we can easily find the precise applicability of the circuit in different VLSI systems. The analysis and comparison provides the better performance of DG-MOSFET based 6T SRAM over Bulk SRAM with Sleep Transistor technique so that is the reason which gives an upper hand to DG MOS based SRAM with Sleep Transistor technique for getting low power dissipation.

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Figure 7 shows the circuit of the bulk 6T SRAM cell and Figure 8 shows the proposed DG-MOSFET based 6T SRAM cell. Figure 9 depicts the transient response while Figure 10 shows response of the proposed DG-MOSFET based 6T SRAM cell by cadence virtuoso tool using the process technology at 90nm, with the minimum supply voltage 0.7V.

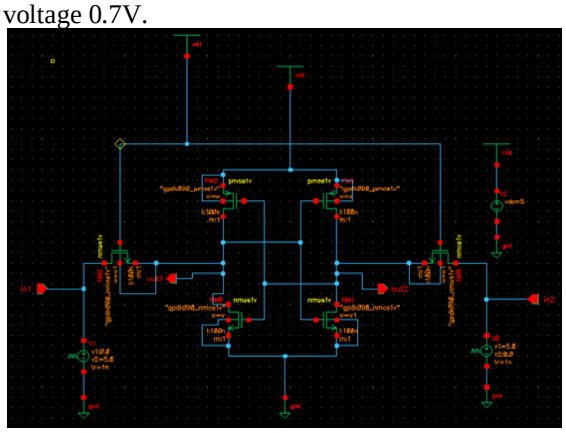

Figure.5 Circuit of the basic 6T SRAM Cell.

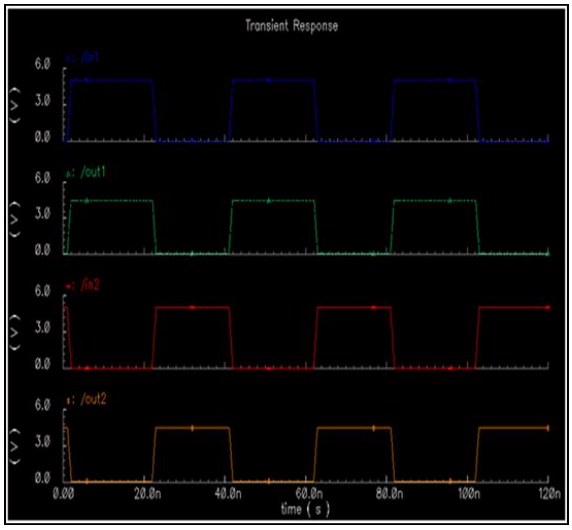

Figure.6 Circuit of the DG-MOSFET Based 6T SRAM Cell with Sleep Transistor.

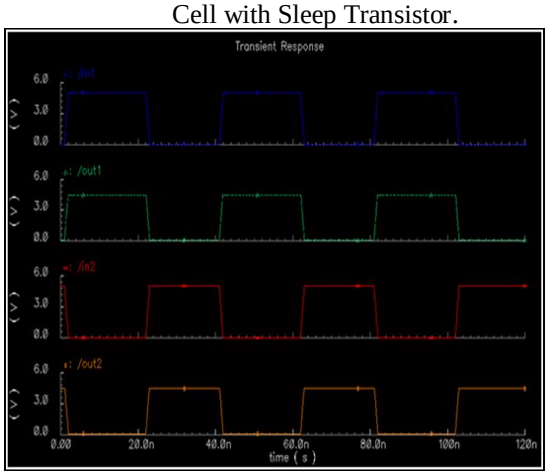

Figure.7 Transient Response of the bulk SRAM Cell.

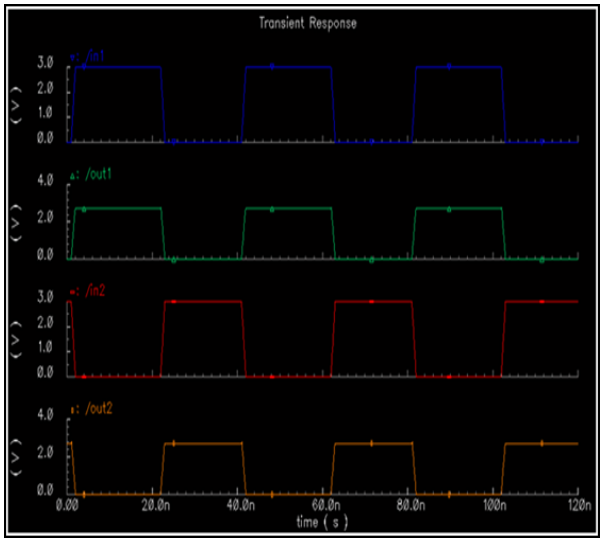

Figure.8 Transient Response of the Proposed DG-MOSFET Based 6T SRAM Cell with Sleep Transistor

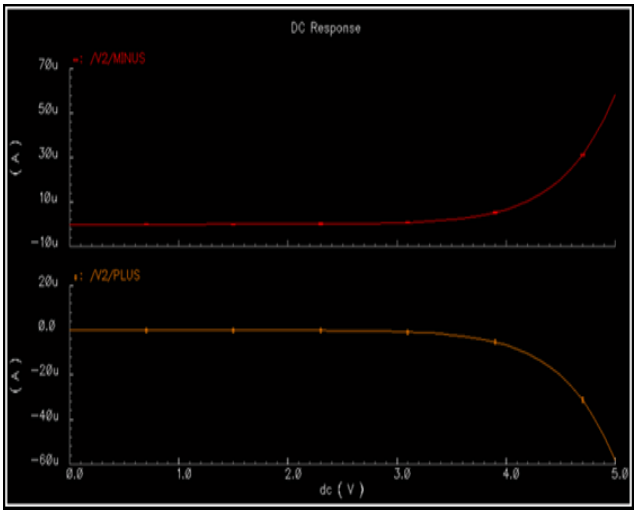

Figure.9 DC Response of the bulk SRAM Cell

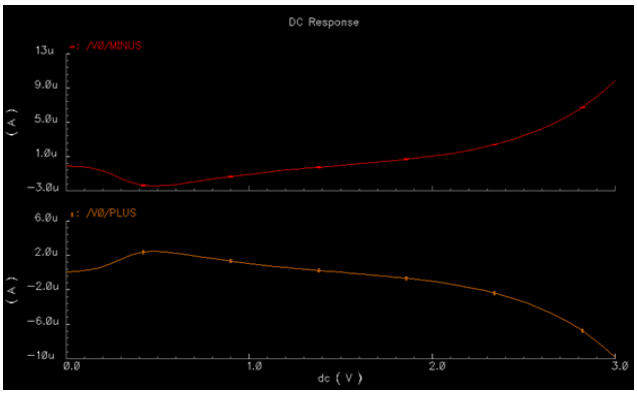

Figure.10 DC Response of the Proposed DG-MOSFET Based 6T SRAM Cell with Sleep Transistor

Figures 7 and 8 depict the transient response. The transient response shows that the bulk 6T SRAM works well as it stores 1 bit of data according to the input pulse range. In

the diagram four waveforms are shown. First waveform is the input to the SRAM of the range 0 to 5V for 120ns. The second waveform is the output of the first waveform which is same as input and provide accurate information to the output. The third waveform is the second input to the SRAM of the range 5 to 0V for 120ns. The fourth waveform is the output of the first waveform which is same as second input but invert of the first input which is required according to the functionality of the SRAM.

It can be observed from the results that the DGMOSFET-based 6T SRAM stores 1 bit of data within the input pulse range. First waveform is the input to the DG-MOSFET based 6T SRAM of the range 0 to 3V for 120ns. The second waveform is the output of the first waveform which is same as input and provide accurate information to the output. The third waveform is the second input to the DG-MOSFET based 6T SRAM of the range 3 to 0V for 120ns. The fourth graph indicates the output of the first graph input but invert of the first input which is required according to the functionality of the SRAM.
From the transient response, it can be observed that the circuits work well and the function of the SRAM are perfect in both of them. Figures 9 and 10 depict the dc response. From the dc response, it is observed that the applied DC voltage to the circuit is 5V. The outputs rendered are from opposite polarity terminals of the supply.

For the DGMOSFET based SRAM, the applied DC voltage to the circuit is 3V. The graphs are again obtained from opposite polarity terminals of the supply. Further the overall leakage value was observed. As we know that the leakage current is the sum of diffusion and subthreshold current so that the waveforms we are getting from the circuits are given the combined value of the both. For calculating the leakage current of the circuit, the sleep transistor is customarily connected adjacent to the ground terminal to estimate the net leakage of the circuit, as it is the final path to the ground terminals for the leakage current to flow right from the source node to the ground node.
The comparison table of leakage current for the different values of MOSFET width is given below:

Table 1: Leakage current values with Sleep Transistor at 90nm technology

W/L = x/100	AT THE SOURCE NODE OF	BULK 6T SRAM	DG-MOSFET BASED 6T SRAM
x = 450nm	NMOS	508.20pA	19.101pA
x = 500nm	NMOS	548.46pA	20.557pA
x = 550nm	NMOS	587.76pA	22.057pA
x = 600nm	NMOS	628.40pA	23.519pA
x = 650nm	NMOS	668.78pA	25.016pA

W/L = x/100
AT THE SOURCE NODE OF BULK 6T SRAM DG-MOSFET BASED 6T SRAM
x = 450nm NMOS 508.20pA19.101pA
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x = 550nm NMOS 587.76pA22.057pA
x = 600nm NMOS 628.40pA23.519pA
x = 650nm NMOS 668.78pA25.016pA

From the Table 1, we can observed that by using different feature sizes, we can get different values of the leakage current. As the width of the MOSFET of the bulk 6T SRAM is increased, the leakage current is reduced. The same is done with the DG-MOSFET based SRAM. When we compare the values of leakage current of the bulk 6T SRAM with DG-MOSFET based 6T SRAM, reduction in the leakage current is found which is depicted by the corresponding waveforms.

IV. CONCLUSION

From previous discussions, it can be inferred that leakage reduction is critical in case of almost all memory elements. A 6T SRAM has been designed using the 90nm DG MOS and Sleep Transistor for leakage reduction. The transient, DC and parametric analysis provide the results. The transient, DC, and parametric analyses have been conducted as part of the experimental results. The parametric analysis gives different values of leakage current on different width of the MOSFET which shows that the bulk 6T SRAM consumes more power than DG-MOSFET based 6T SRAM with Sleep Transistor. A comparative leakage current analysis with respect to the bulk 6T SRAM indicates the fact that the proposed SRAM design outperforms the existing approach in terms of leakage current and hence implies lesser power dissipation for the circuit.

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