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Self-Repairable Multiplexer in Real Time for Fault Tolerant Systems

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Abstract- As a result of VLSI, more transistors can be packed onto a single chip. The system or chip is more likely to malfunction when the distance between transistors or circuits decreases. Fault-tolerant systems are crucial for preventing inaccurate conclusions. A multiplexer is an apparatus that selects one or more input signals based on another signal. Only self-verifying multiplexers have been the sole focus of prior writings. In this research, we present a 2:1 multiplexer that can fix both permanent and transient mistakes on its own. Two distinct architectures for a self-repairing multiplexer are introduced. The multiplexer mistake is corrected in the first design by means of supplementary circuitry. In the second design, the multiplexer's construction blocks including OR and AND gates are self-repairing. These self-healing multiplexer layouts can recognize and fix both single- and multiplexer-level problems. These self-healing multiplexer layouts are able to identify and fix a wide variety of errors. All errors can be recovered in the proposed designs. The Cadence tool verifies the circuits' functionality. Mentor graphics CMOS Technology at 45nm was used to verify the aforementioned project.

Keywords- VLSI, Fault, Error, Self-checking, Self-repairing.

I. INTRODUCTION

The response of a circuit may be invalid due to the presence of faults. This produces untrustworthy results. To withstand faults, fault-safe systems are essential. As a result, self-checking and self-repairing are required for the circuit to function effectively. In self-checking, the circuit discovers the problem on its own, and in self-repairing, the circuit may repair itself and deliver the desired output.

Individual circuit gates have an impact on how well a circuit functions as a whole. Using fewer gates in your design may enhance performance in terms of delay, area, and power. To attain high speed, the crucial path should be as short as possible. Similarly, fewer gates are used at the circuit level to obtain low power without affecting the accuracy of the circuit. A wide range of applications, such as adders, multipliers, communication, and so on. The multiplexer will choose the input data and send it to the output based on the selection signal. When a multiplexer fails, incorrect data is generated. The multiplexer must be fault secure in order to deliver correct data even when there are problems.

II. EXISTING SYSTEM

The present model uses 65nm technology to create the entire adder, which comprises of AND, OR gates, and a 2X1 MUX. In the existing method, the factors in terms of power, delay, and power delay product are optimized in high speed, and the average power consumed is very high, and the power delay product is greater, the noise margin is greater, and other factors such as drive capability are greater. To address these issues, we will propose a model with 45nm technology.

AND Gate simulation with and without incorrect occurrence. There might be a problem with the multiplexer. This may result in incorrect findings; hence fault-free design is particularly important for detecting flaws. The performance of the system is determined by the gates employed in the circuit design. By adopting constrained gates, the suggested design's performance in terms of power PDP and latency may be improved. The simulation of OR Gate with and without fault a logic operation that returns one if at least one operand returns one and returns zero else this is a without fault in with fault inverse of OR Gate.

III. PROPOSED SYSTEM

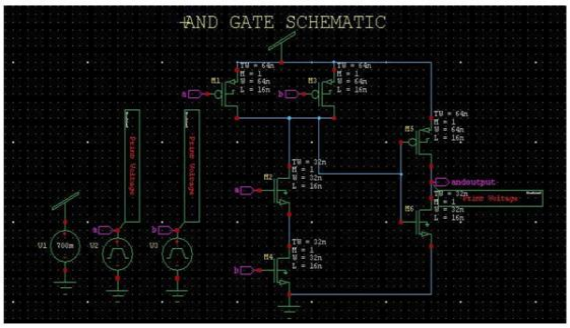

Fig 1. Schematic of AND gate without fault.

The AND gate schematic, which is a blend of PMOS and NMOS logic, is designed in 65nm technology. Tanner S-EDIT Tool was used to create it.

The following image depicts the design for a faulty AND gate, which includes a number of PMOS and NMOS logic units. It was built with 65nm technology. It was made with the S-EDIT Tool.

The accompanying simulation picture shows that with the inputs A=0 and B=0, the output is 0. If A=0, B=1, the outcome is 0.If A=1 and B=0, the result is 0.If A=1, B=1, the result is 1. As a result, assuming there is no defect in the AND gate, the output will be the value of y.

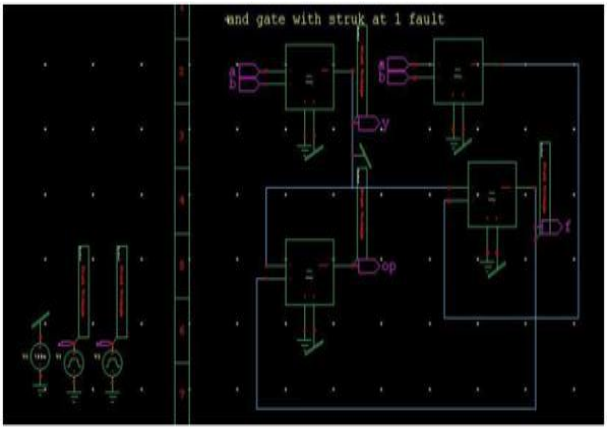

Fig 2. Schematic of AND gate with fault.

According to the simulation picture above, whenever the inputs A=0, B=0, the output is fault at y and the output is 0. If A=0 and B=1, the output is fault at and 0. If A=1 and B=0, the output at y is fault and the output is 0. If A=1, B=1, the output is incorrect and is 1. We can see from the simulation graphic above that if the AND gate fails the output is the inverse of y.

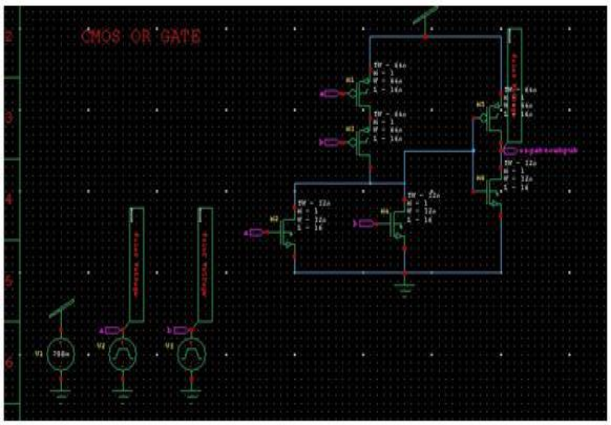

Fig 3. Schematic of OR gate without fault.

The above graphic depicts the simulation results of a problem-free OR gate. To simulate it, the CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool is employed. W-EDIT is a programmed that analyses wave forms.

From above simulation figure it is observed that whenever the inputs A=0, B=0, the output is 0. If A=0, B=1,The output is1.IfA=1,B=0, The output is 1 .If A=1, B=1, The output is1.

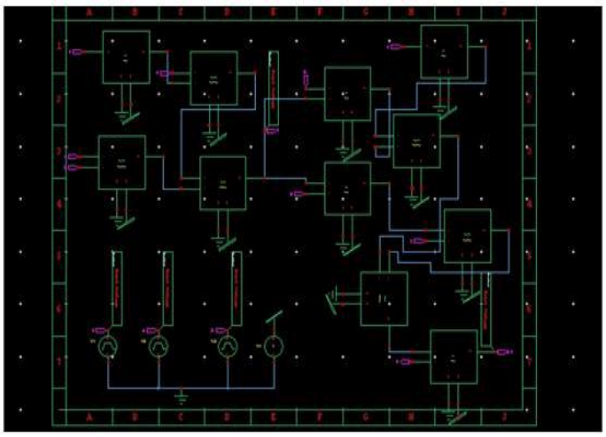

Fig 4.Schematic of OR gate with fault.

The schematic of a defective OR gate, which is a mix of PMOS and NMOS logic constructed in 65nm technology, is shown above. Tanner S-EDIT fig 5 2x1 multiplexer is used in its design.

The inverter is often regarded as the most fundamental logic gate, performing a Boolean operation on a single input variable. The symbol, truth table, and overall construction of a CMOS inverter are seen in Fig.1. The basic structure illustrated consists of a PMOS transistor at the panda MOS transistor at the bottom. CMOS is also known as complementary-symmetry metal-oxide-semiconductor.

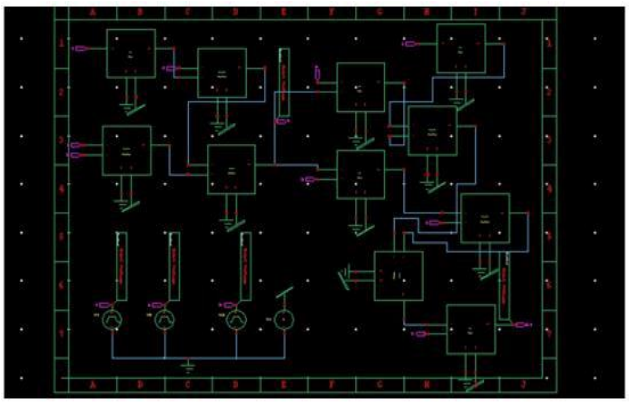

Fig 5. Schematic Of 2X1 MUX without fault.

According to the simulation picture above, whenever the selection line is 0inputs A=0, B=0, the output is fault at Y, and the output is 0. If A=0 and B=1, the output at Y is fault and the output is 0. If A=1 and B=0, the output is fault at Y and 1. If A=1 and B=1, the output is a fault at Y

and a 1. When the selection line is 0, the output simply follows A's input.

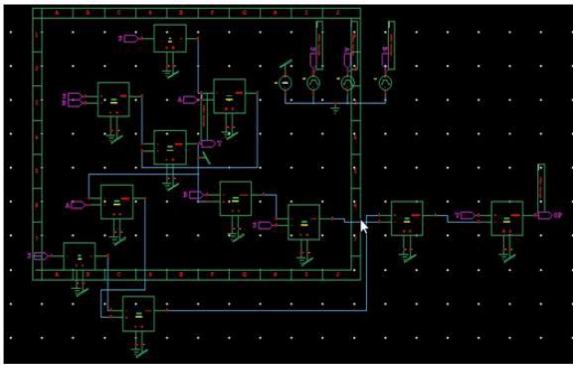

Fig 6. Schematic Of 2X1 MUX with fault.

The diagram of a defective 2X1 MUX, which is a mix of PMOS and NMOS logic constructed in 65nm technology, is shown above. Tanner S-EDIT Tool was used to create it.

When the selection line is 1, the inputs A=0, B=0, and the output is fault at Y and 0. If A=0 and B=1, the output is a fault at Y and a 1. If A=1 and B=0, the output is fault at Y and zero. If A=1, B=1, the output is 1 and the output is fault at Y. That is, whenever the selection line is 1, the output simple follows the input of B.

IV. RESULTS

The below figure shows the power analysis of AND gate. It analyzed by using tanner tool. The average power consumed around 4.57e-04 watts. Max power 3.20e-04 Minimum power consumed around 3.41e-05 watts. For above simulation have done with 5V

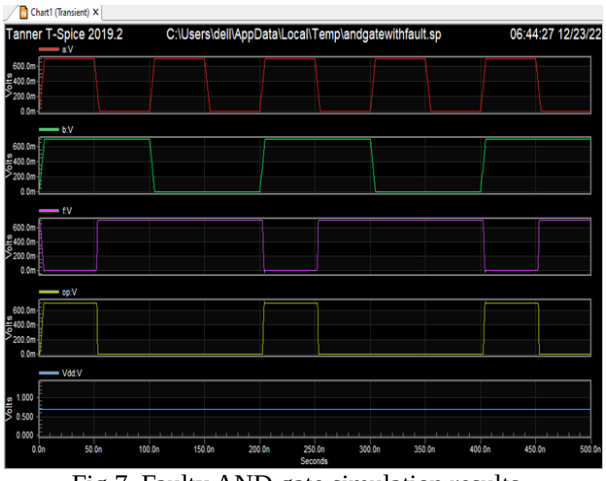

Fig 7. Faulty AND gate simulation results.

It analyzed by using tanner tool. The time delay is 150.65n and figure shows the PDP analysis of AND gate. It analyzed by using tanner tool. The PDP is 688.47. For above simulation have done with 5VDD.

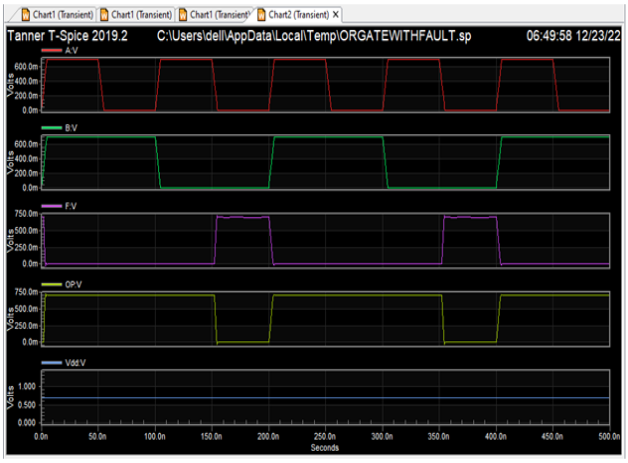

Fig 8. Simulation of Faulty OR gate.

The below figures shows the power analysis of OR gate. It analyzed by using tanner tool. The average power consumed around 9.85 e-05 watts. Max power 2.86 e-04 Minimum power consumed around 5.60e-05. For above simulation have done with 5VDD. It analyzed by using tanner tool. The time delay is 250.13n. It analyzed by using tanner tool. The PDP is 2463.78.

Fig 9. Simulation of Faulty2x1Multiplexer.

Existing technology with 65nm				Proposed technology with45nm		
	Power (W)	Delay (ns)	PDP	Power (W)	Delay (ns)	PDP
AND	4.57	150.65	688.47	1.33	100.17	133.22
OR	9.85	250.13	2463.7	7.22	200.17	1445.2
MUX	90.92	70.87	6443.5	1.36	50.53	68.72

The above figure shows the power analysis of2X1 MUX. It analyzed by using tanner tool. The average power consumed around 90.92e-04 watts. Max power 86.12e-04 Minimum power consumed around 87.05e-05 watts. For above simulation have done with 5VDD. It analyzed by

using tanner tool. The time delay is 70.87n. It analyzed by using tanner tool. The PDP is 6443.50

V. CONCLUSION

Because the multiplexer is crucial to many systems, malfunctions in the multiplexer might cause those systems to produce erroneous results. To prevent errors, fault tolerant systems require a multiplexer that is also fault tolerant. The proposed self-repairing multiplexers find application in multi-bit arithmetic and arithmetic operations such as multiplication and addition.

The proposed self-repairing multiplexers can be employed in fault-tolerant systems for complete error recovery. In other words, the structure can fix itself without any help from outside sources. In doing so, you'll stay out of the way of the above obstruction. This is done by simulating the circuits and checking their results. This study confirms the proposed structures' fault tolerance

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