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Design of Efficient BCD Adders Correction Logic in QCA Technology

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Abstract- Recent experiments in the field of VLSI designing and Nanotechnology have demonstrated a working cell suitable for implementing the Quantum-dot Cellular Automata (QCA). QCA is a transistor less computational model which is expected to provide high density nanotechnology implementations of various CMOS circuits. QCA has been constrained by the problem of meta-stable states. QCA adder with comparatively less number of cells and area has been proposed in this project. This paper also demonstrates a reversible logic synthesis for one bit adder which gives a superior solution for side channel attack based on power analysis in security applications. The new proposed hybrid method reduces cell counts and area and uses conventional form of QCA cells. QCA implementation provides efficient design methodology for faster speed, smaller size and low power consumption when it compared to technology imposed by transistors. QCA provides ability to quickly layout a QCA design by providing an extensive set of CAD tools.

Keywords- QCA (Quantum-dot Cellular Automata), QCA cell, One bit BCD adder, power, area, faster.

I. INTRODUCTION

A quantum-dot cellular automaton (QCA) has been recognized as one of the technologies that may replace field-effect transistor (FET)-based computing devices at the Nano scale level. Current complementary metal oxide semiconductor technology is going to approach a scaling limit in deep nanometer technologies.

The current silicon transistor technology faces challenging problems, such as high-power consumption and difficulties in feature size reduction. Nanotechnology is an alternative to these problems, and the international technology road map for semiconductors (ITRS) report summarizes several possible technology solutions.

A Quantumdot cellular automaton (QCA) is a nanotechnology that offers a new method of computation and information transformation.Nanotechnology draws much attention from the public now-a-days. Because the current silicon transistor technology faces challenging problems, such as high power consumption and difficulties in feature size reduction, alternative technologies are sought from researchers.

A quantum-dot cellular automaton (QCA) is one of the promising future solutions. Since it was first introduced in 1993, experimental devices for semiconductor, molecular, and magnetic approaches have been developed. Quantum dot cellular automata, which is an array of coupled quantum dots to implement Boolean logic functions. The advantage of QCA is high packing densities due to the small size of the dots, simplified interconnection and low area delay product.

Quantum-dot cellular automata (QCA) is an attractive emerging technology suitable for the development of ultra-dense low-power high-performance digital circuits for this reason, in the last few years, the design of efficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits with the main interest focused on the binary addition that is the basic operation of any digital system of course.

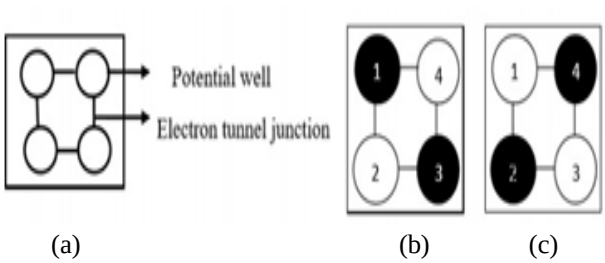
In QCA technology is part of the quantum physics and two major gates are present in it .Those are inverter and majority gate by using these gates we can design digital circuits. The BCD adder requires correction logic after the sum exceeds more than nine; the correction logic is designed with the minimum number of gates using the majority gate and inverter gates.

1. QCA Cell:

A new physical structure for a digital design that offers novel computing architecture is Quantum-Dot Cellular Automata (QCA) technology. Therefore, QCA cell is locked with two electrons, which exist in the potential wells in diagonal positions because of the Coulombic repulsion. The potential wells are linked through the electron tunnel junctions as shown in Figure 1.1(a).

The tunnelling of electrons between the potential wells is achieved by the application of the suitable potential. The positions of diagonally occupied two mobile electrons

represent binary information as logic ‘0’ and logic ‘1’ as shown Figure 1.1 (b) and 1.1(c) respectively



(a) (b) (c)

Fig 1. (a) QCA cell (b) QCA logic 0 (c) QCA logic 1.

2. QCA Wire:

A series of cells can be used as interconnection wire as shown in Figure 2.1. The propagation of the signal from one end (input) to the other end (output) takes place because of Coulombic repulsion between the adjacent cells. As the computations in QCA technology is performed using an array of the quantum devices the inner cells have no direct contact; so the information or energy can pass in the array only from the edges.

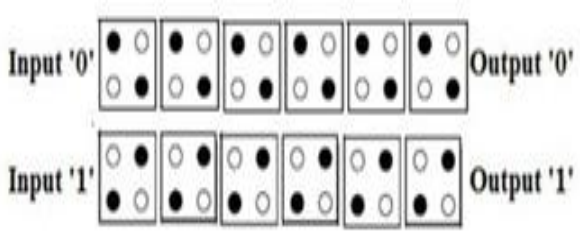


Fig 2. QCA Wire.

3. QCA Inverter:

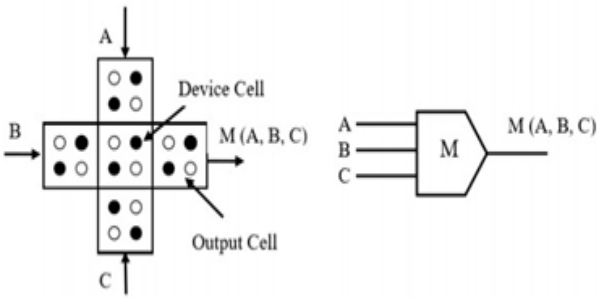
QCA inverter can be implemented in two ways positioning and rotation of cells are shown in Figure 2.2. The different polarization of QCA cells and the electrostatic interaction between the cells is inverted. Figure 2.2 (a) shows one way to position QCA cells to invert the output from input logic level. Figure 2.2 (b) indicates the way in which successive cells alternate the logic level. The quantum dots in cells are rotated by 45 degree. Figure 2.2 (c) shows the most robust way to construct the inverter.

(a) (b) (c)

Fig 3. (a) Two cell inverter (b) Rotated inverter cell (c) Robust QCA inverter.

4. QCA Majority gate:

The basic logic primitives in QCA technology are comprising three input majority gate (M) and an inverter. The majority gate structure and its symbol are shown in Figure 2.3(a) and 2.3(b). The logic function realized by majority gate is M(A,B,C)= AB+BC+CA



(a) (b)

Fig 4. (a) Majority gate (b)Majority gate symbol.

The majority gate needs five cells to propagate majority of ‘1’ to the output. Three polarizations of input lines converge at a device cell, whose state is determined.

II. LITERATURE REVIEW

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded, decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder– subtractor.

Other signed number representations require a more complex adder.Adders are fundamental circuits for most digital systems and several adder designs in QCA have been proposed, and a performance comparison was improved. Better adder performance depends on minimizing the carry propagation delay and reducing the area.

In 1993, Lent et al. proposed a physical implementation of an automaton using quantum dot cells. The automaton quickly gained popularity and it was first fabricated in 1997. Lent combined the discrete nature of both cellular automata and quantum mechanics, to create nanoscale devices capable of performing computation at very high switching speeds and consuming extremely small amounts of electrical power. Today, standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm.

Quantum dot Cellular Automata are based on the simple interaction rules between cells placed on a grid. A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them. Because of Coulombic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations P) determine two possible stable states that can be associated to the binary states 1 and 0.

Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality.The basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. The physical mechanism for interaction between dots is the Coulomb interaction and the quantum-mechanical tunneling. Electrons are able to tunnel between the dots, but they cannot leave the cell. If two mobile electrons are placed in the cell.

III. METHODOLOGY AND METHODS

1. Methodology:

The main objective of this paper is to perform both BCD addition and BCD subtraction in a single circuit with minimum number of garbage gate count and constant input. To achieve the operation of reversible BCD addition and subtraction in a single circuit two new gates are proposed which are optimized such that it doesn't possess any restrictions of reversible gates as mentioned above. It has been proved that the proposed reversible BCD arithmetic circuit is better than the existing logics in the literature; in terms of number of garbage outputs, constants inputs And BCD or Binary Coded Decimal is that number system or code which has the binary numbers or digits to represent a decimal number. A decimal number contains 10 digits (0-9).

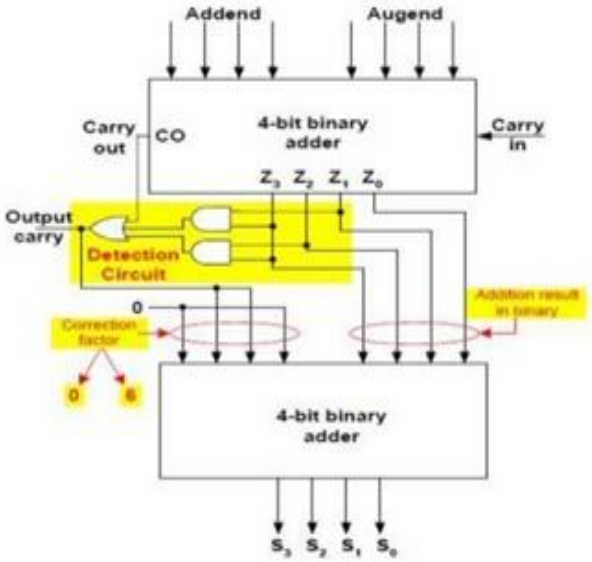


Fig 5. One Digit BCD adder.

Now the equivalent binary numbers can be found out of these 10 decimal numbers. In case of BCD the binary number formed by four binary digits, will be the equivalent code for the given decimal digits. In BCD we can use the binary number from 0000-1001 only, which are the decimal equivalent from 0-9 respectively. Suppose if a number have single decimal digit then its equivalent Binary Coded Decimal will be the respective four binary digits of that decimal number and if the number contains two decimal digits then its equivalent BCD figure 3.1 will be the respective eight binary of the given decimal number. Four for the first decimal digit and next four for the second decimal digit. It may be cleared from an example.

2. QCA BCD Adder:

A Binary Coded Decimal (BCD) adder is a circuit which adds two 4-bit BCD numbers in parallel and produces a 4-bit BCD result. Fig. 1 shows the block diagram of conventional BCD adder. The circuit must include the correction logic to produce valid BCD output. Two 4-bit BCD numbers X and Y along with carry input is added using conventional 4-bit parallel adder, 4-bit sum and a carry is taken out. If the carry output is set or if the result is greater than nine, binary 0110 is added to the intermediate sum output with the help of second stage 4-bit parallel adder circuit.

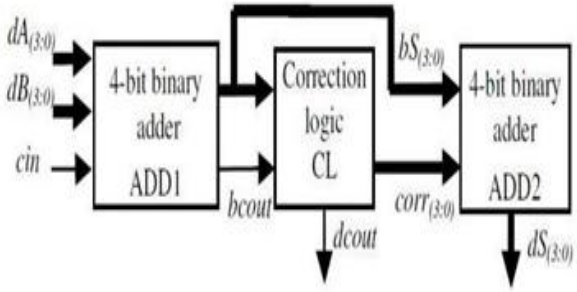


Fig 6. BCD adder using QCA.

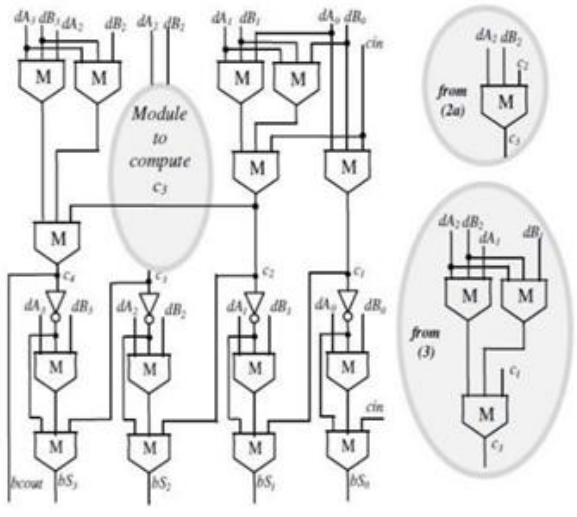


Fig 7. New BCD adder.

To understand the new design strategy, let's examine first the 4-bit binary adder ADD1. It receives the digits dA(3:0) and dB(3:0) and the carry cin as inputs, and computes the binary results bcout and bS (3:0). Demonstrates that, for QCA-based rippling adders, the optimal logic structure for propagating a carry Ci through a single bit position is represented by that introduces only one MG between Ci and Ci+1.

3. Materials:
The many-sided excellent of VLSI is being planned and applied nowadays makes the manual way to deal with outline unfeasible. Outline mechanization is the request of the day. With the quick mechanical improvements over the maximum recent two many years, the reputation of VLSI.

4. Large Scale Integration:
Advance improvement, pushed with the aid of the identical economic variables, precipitated "widespread scale incorporation" (LSI) within the mid Seventies, with a large number of transistors in line with chip. Coordinated circuits, for instance, 1K-bit RAMs, including gadget chips, and the main microchips, that began to be fabricated in direct amounts in the mid 1970s, had under 4000 transistors. Genuine LSI circuits, shifting in the direction of 10,000 transistors, commenced to be created around 1974, for PC number one reminiscences and second-era chip.

IV. XILINX ISE OVERVIEW

The Integrated Software Environment (ISE) is the Xilinx design software suite that allows you to take your design from design entry through Xilinx device programming. The ISE Project Navigator manages and processes your design through the following steps in the ISE design flow.

1. Design Entry:
Design entry is the first step in the ISE design flow. During design entry, you create your source files based on your design objectives. You can create your top-level design file using a Hardware Description Language (HDL), such as VHDL, Verilog, or ABEL, or using a schematic. You can use multiple formats for the lower-level source files in your design

2. Synthesis:
After design entry and optional simulation, you run synthesis. During this step, VHDL, Verilog, or mixed language designs become netlist files that are accepted as input to the implementation step.

3. Implementation:
After synthesis, you run design implementation, which converts the logical design into a physical file format that can be downloaded to the selected target device. From Project Navigator, you can run the implementation process in one step, or you can run each of the implementation processes separately. Implementation processes vary depending on whether you are targeting a Field Programmable Gate Array (FPGA) or a Complex Programmable Logic Device (CPLD).

4. Verification:
You can verify the functionality of your design at several points in the design flow. You can use simulator software to verify the functionality and timing of your design or portion of your design. The simulator interprets VHDL or Verilog code into circuit functionality and displays logical results of the described HDL to determine correct circuit operation. Simulation allows you to create and verify complex functions in a relatively small amount of time. You can also run in- circuit verification after programming your device.

After generating a programming file, you configure your device. During configuration, you generate configuration files and download the programming files from a host computer to a Xilinx device.

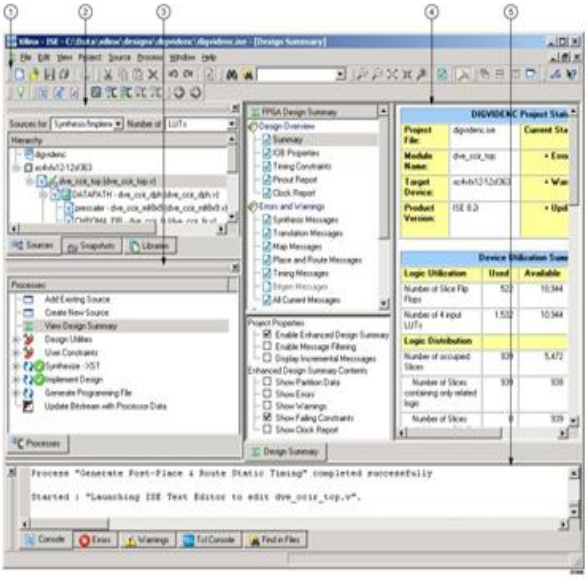


Fig 8. Project Window.

- Toolbar
- Sources window
- Processes window
- Workspace
- Transcript window

5. To create a project:
- Select File > New Project.
- In the New Project Wizard Create New Project page
- Click Next.
- If you are creating an HDL or schematic project, skip to the next step. If you are creating an EDIF or NGC/NGO project, do the following in the Import EDIF/NGC Project page

- If you are creating an EDIF or NGC/NGO project, skip to If you are creating an HDL or schematic project.
- Click Next, and optionally, add existing source file to your project in the Add Existing Sources page.
- Click Next to display the Project Summary page.
- Click Finish to create the project

6. To Open Project an Example:

- Select File > Open Example.
- In the Open Example Project dialog box, select the Sample Project Name that you want to use. To help you choose an example project, the Project Description field describes each project. In addition, you can scroll to the right to see additional fields, which provide details about the project.
- In the Destination Directory field, enter a directory name or browse to the directory.
- Click OK.

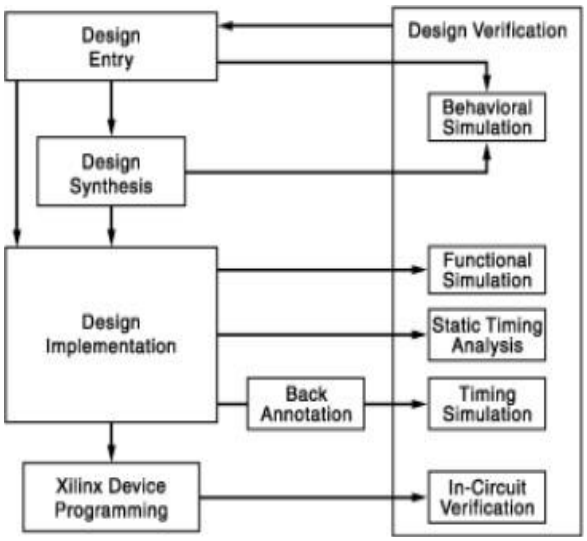


Fig 9. Design Overview.

V. SIMULATION RESULT

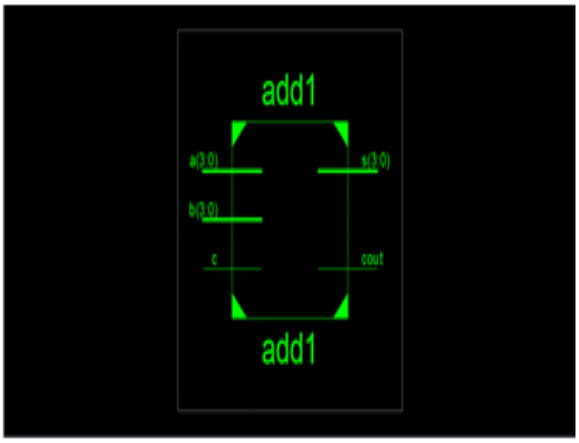


Fig 10. BCD adder schematic diagram.

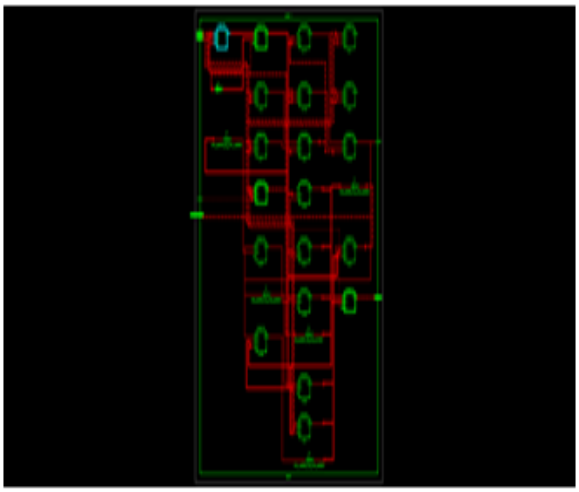


Fig 11. RTL diagram.

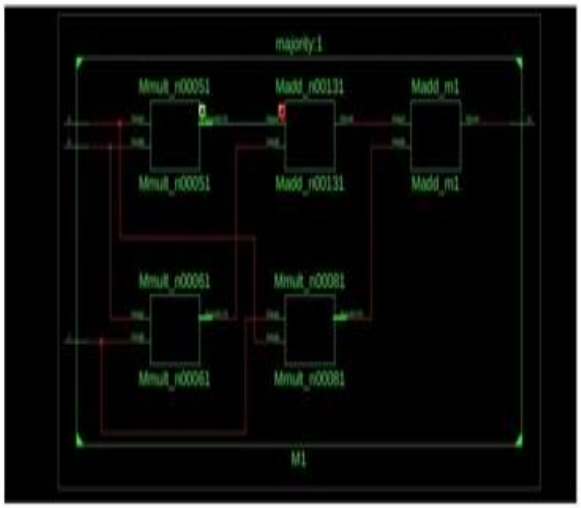


Fig 12. Internal Logical Circuit.

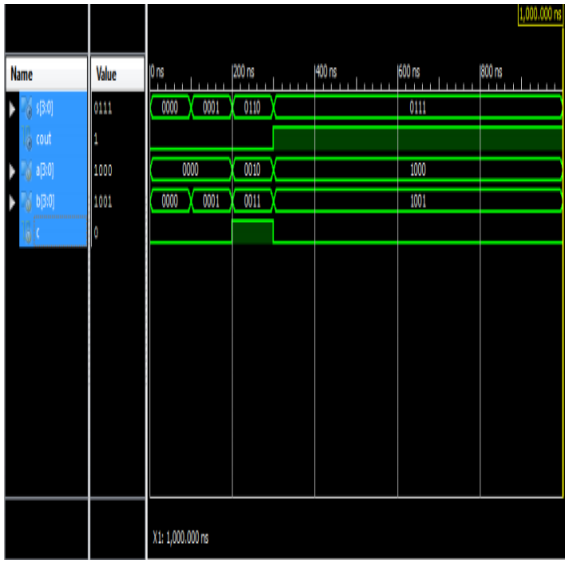


Fig 13. Timing diagram of BCD adder.

VI. DISCUSSIONS

The design parameters can be known by the synthesis Report Netlist, Design summary and Timing Report and Timing summary. The design summary gives information about the design completely regarding area and power details.

1. Design Summary:
Top Level Output File Name: add1.ngc Primitive and Black Box Usage
BELS = 20
GND = 1
LUT2 = 1
LUT3 = 3
LUT4 = 2
LUT5 = 9
LUT6 = 3
VCC = 1
IO Buffer = 14
IBUF = 9
OBUF = 5
DSPs =8
DSP48A1 = 8

2. HDL Synthesis Report:
Macro Statistics Multipliers = 8
1x1-bit multiplier =8
Adders/ Subtractors =4 1-bit adder = 8

3. Timing Summary:
- Speed Grade: 3 macros seconds Minimum period: No path found
- Minimum input arrival time before clock: No path found Maximum output required time after clock: No path found Maximum combinational path delay: 17.130ns
- Total = 17.130ns (11.541ns logic, 5.589ns route) (67.4% logic, 32.6% route)

VII. CONCLUSION

A new design approach has been presented and demonstrated to achieve efficient QCA-based implementations of decimal adders. Unconventional logic formulations and purpose- designed logic modules here proposed allows outperforming decimal adders known in literature. In fact, the new 1-digit BCD adder exhibits computational delay and area occupancy and lower than existing competitors. These advantages become even more evident when two n-digit decimal numbers must be summed.

. FUTURE SCOPE

The proposed BCD adder is a implement n-digit BCD Adder using QCA can achieve high device density, extremely low power consumption, and very high switching speed Modelling Physical Systems Example: Spin Chains Quantum Computation Example : Coloured QCA . . . . .

Single Spin Measurement Example: Physical Implementation Methodology We can design the any digital circuit with only two gates majority and inverter gate design of ALU, Multiplexers, shift registers ,memory circuit implementation also possible the QCA technology.

IX. ACKNOWLEDGEMENT

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