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Design of Low Power Multiplier with Improved Column Bypassing Scheme

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Abstract- In design of portable electronic devices for signal processing applications the primary constraints are Power, speed and area. Multiplier plays a vital role in DSP applications. In this paper, a high speed and low power multiplier with improved column bypassing scheme is presented. Primarily power reduction is achieved by disabling the supply voltage applied to non-functional blocks when the operands of the multiplicands are 0. Power reduction is obtained by both architectural and circuit level modifications. The proposed multiplier is involved with a new adder architecture which is also responsible for reducing the power consumption and propagation delay. Simulated results are obtained with UMC (United microelectronics Corporation) 90nm and 0.9V CMOS technology with help of cadence spectre simulation tool. The proposed multiplier has been compared with popular multipliers and performance parameters such as speed, power dissipation and area occupation are found better. The proposed multiplier is holding a better choice for the low frequency (≤ 50 MHz) applications. From the obtained results for randomly generated input test patterns having uniform distribution probability and power saving would be more if operands have more 0's than 1's.

Keywords- Multipliers, Power, Area, Speed, UMC, Cadence etc.

I. INTRODUCTION

In the modern scenario it is require to design the systems with less complexity, low power [1-5] consumption and high speed over the years there have been so many techniques proposed for reduction of power consumption. All these techniques have their own merits and demerits. Traditional techniques as reached its saturation and there is a necessity for the exploration of new techniques. With the increasingly stringent demands on battery space and weight in portable multimedia devices, there exists a strong necessity to investigate techniques for lowering energy dissipation.

1. Power Dissipation:
The sources of power consumption in digital CMOS circuits are static power dissipation and dynamic power Eq. (1) shows power consumption of digital CMOS circuits.

$$P_{total} = \alpha f C_L V_{DD}^2 + I_{sc} V_{DD} + I_{leakage} V_{DD} \quad \text{Eq. (1)}$$

Where α is switching transition of a clock cycle, CL is the output capacitance, VDD is the supply voltage and f is the switching frequency which is fixed in many DSP and dedicated applications, ISC is the short circuit current, and Ileakage the leakage current. In the submicron technology, leakage current is a predominant contributor of the power consumption. Circuit and technology level techniques used dual Vt partitioning, multi-threshold CMOS and power gating approach to reduce the leakage power.

2. Power Gating Technique:
Power gating approach can reduce both the components of power dissipation up to a good extent. In this project, power gating approach is considered for the power reduction of proposed multiplier. This technique uses sleep transistors to shut down the supply of the selective logic blocks which are not functional during bypassing operation. PMOS transistor acts as a header switch to connect the supply voltage VDD to logic block and NMOS acts as a footer switch to connect the ground to the logic block as shown in figure 1.1. The proposed multiplier utilizes power gating approach.

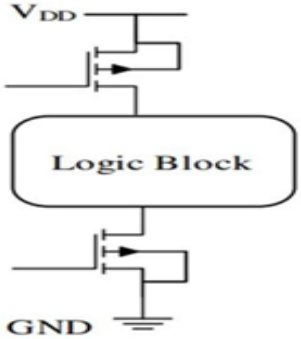

Fig 1. Power gating technique.

Multipliers [6, 7] are basic arithmetic operations used in virtually all applications involving digital signal processing [7-10]. Early multiplier designs focus on pursuing high speed operation or low circuit complexity. However, with the advance of VLSI technology, the computation speed can be improved at a constant pace. Instead, power/energy consumption has become a more and more prominent design factor under the prevailing of battery-operated mobile devices.

In this project, multiplier adopts improved column bypassing scheme and new adder architecture for better overall performance.

3. Multiplier:

An efficient multiplier should have following characteristics Accuracy: good multiplier should give correct result.

- **Speed:** Multiplier should perform operation at high speed
- **Area:** A multiplier should occupy less chip area
- **Power:** Multiplier should consume less power

Multiplication process has three main steps:

- Partial product generation.
- Partial product reduction.
- Final addition.

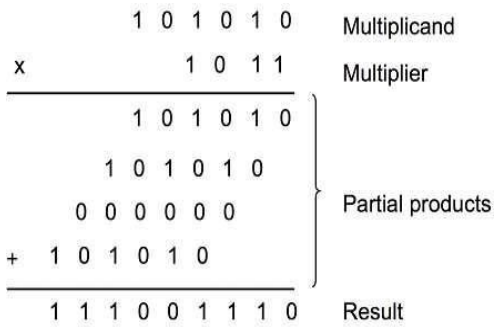

Fig 2. Multiplication process.

For the multiplication of an n-bit multiplicand with an m-bit multiplier, m partial products are generated and product formed is n+m bits long. Multiplication is the basic operation performed by many common DSP functional unit such as FIR filters and FFT modules. Reduction in the power consumption of the multiplier can reduce a significant portion of the power in the overall digital system. The multiplication of n bit wide numbers A and B is defined as follows.

$$P = A \times B = \sum_{i=0}^{i-1} \sum_{j=0}^{j-1} \left((A_i B_j) 2^{(i+j)} \right) \quad \text{Eq. (2)}$$

Here P represents the products, *A*i is ith bit of multiplicand and *B*j is jth bit of multiplier. A 4x4 basic multiplication is shown in figure 2.2.

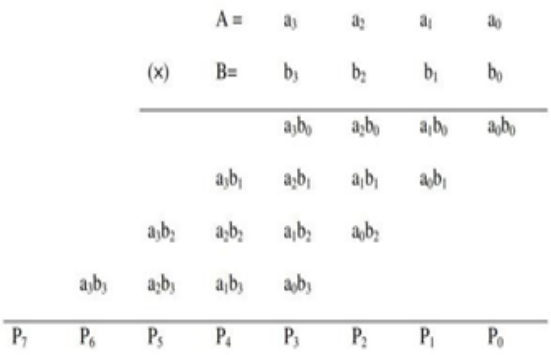

Fig 3. A 4 X 4 basic multiplication.

4. Multiplier types:

Conventionally multipliers are Iterative type multipliers and Array type multipliers. Iterative type multiplier uses same hardware with series of shift and adds operations for computation of multiplication. Reuse of hardware is possible but it requires more clock cycles to initiate addition operation of common hardware. Pipelining is not possible in case of Iterative type multiplier.

Whereas in array type multiplier, pipelining is possible because of repeated, compact and simple structure. Here, the structure is very regular so that layout is favorable for realizing parallel processing. All partial products are generated after one AND-gate delay and are summed up sequentially using array of full adders.

5. Bypassing in multipliers:

Bypassing with reference to multiplier means turning of some columns or rows or both in the multiplier array whenever certain multiplier or multiplicand or both bits are zero. In normal array type multiplier, we have an array of Carry Select Adders/Full Adders. If one of the inputs is zero the sum of adder is nothing but the input other than zero.

Instead of unnecessary addition of zero we can skip the addition and provide input to the next level. In that condition it is beneficial to bypass the other input to the sum. Here addition operation is not required to derive the sum output. The power that is saved here is unnecessary addition with zeros.

Types of bypassing schemes are

- Row Bypassing schemes
- Column Bypassing schemes
- Row and column Bypassing schemes

Row bypassing technique bypasses only rows of multiplier but not columns. Similarly, column bypassing technique bypasses columns of multiplier. Bypassing is two dimensional in Row and column Bypassing multiplier and all adders are provided with bypassing hardware. Any row or column can be bypassed if corresponding bit coefficient is zero.

6. Column bypassing multiplier:

Column bypassing multiplier eliminates the extra correcting circuit to skip the full adder cell and also consumes lesser power than braun multiplier at higher frequency of operation. This multiplier consists of rows of carry save adders. The major focus of this multiplier is to reduce the switching transitions required to perform the computations. The adder cell is shown in figure 2.3.

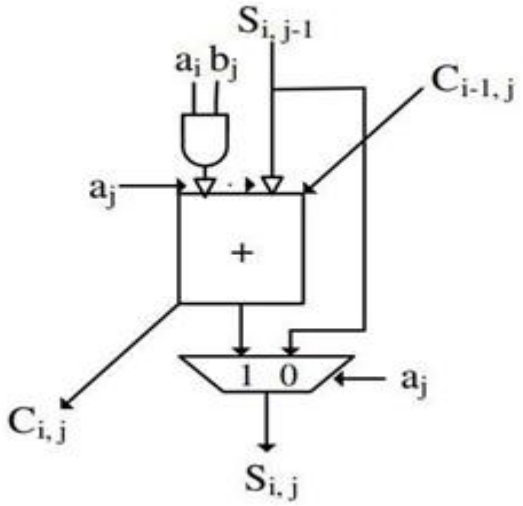

Fig 4. Modified carry save full adder.

Tri-state buffers at the input of the adder cells are inserted for reducing the switching transitions if these cells are bypassed. Whereas, Multiplexer is inserted to select the sum output under no bypassing condition or when the bypassing is used as shown in Fig 3.4. The addition operation in (i-1)th column can be bypassed to (i)th if the corresponding bit in the multiplicand is zero. This operation is performed by disabling adder with buffer under the control of multiplicand bit ai.

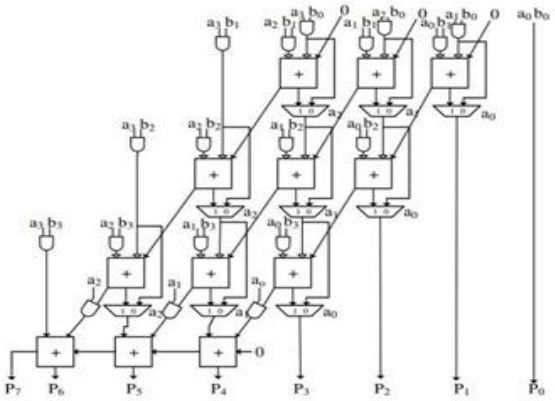

Fig 5. A 4 X 4 Column bypassing multiplier.

The main limitations of this multiplier are its extra hardware cost and power consumption because of buffers, full adder cells and additional AND gates inserted in the last row of adder cells. While simulating, it was observed that this multiplier also dissipates large amount of power than conventional array multiplier due to the buffers if operating at lower frequencies.

7. Modified column bypass multiplier:

Array multiplier consists of rows of adder cells. The sum and carry signals generated from the previous rows are fed into the next rows. Evidently, adders are the major power and area consuming unit of the multiplier.

The power consumption of a multiplier can be lowered by reducing the switching transitions and hardware cost of the adder cells. Switching transitions at the adder cells of the proposed multiplier can be lowered using new improved column bypassing scheme (ICBS) achieved using power gating approach. The proposed multiplier selects the ICBS only if the multiplicand ai is zero as shown in Fig 4.3.

Power gating saves more power by temporarily disabling the supply voltage (VDD) to the selective blocks which are not functional during that period. Therefore, this approach leads to lesser power consumption and area than that of the buffers used by the previous designs. Besides, the performance of buffers is very poor at low frequencies. Hence buffers may not be good choice for low power, low frequency applications.

The occurrence probability of zero in a multiplier can be described by the following equation Eq (3)

$$\sum_{i=1}^{n} prob(D_i)\times\left[\frac{i}{n}\times 50\% + \frac{n-1}{n}\right] + \sum_{i=-1}^{-n} prob(D_i)\times\left[\left|\frac{i}{n}\right|\times 50\% + \left|\frac{n-1}{n}\right|\right]$$

When n is the number of bit in the multiplicand A and multiplier B, Di is the effective data and prob is the probability of specified effective data. Based on the equation (3), the probability of zero in actual multiplier implementation such as adaptive differential pulse code, G723.1 speech code and wavelet-based image coder is over 65%. This is more than uniform distribution probability. This proves that bypassing used in multiplier is much better scheme for power saving. Therefore, the ICBS has been used to design the proposed multiplier.

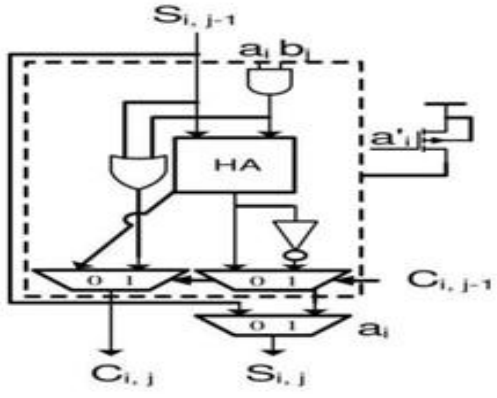

Fig 6. Proposed adder cell.

Secondly, the new adder architecture reduces the power consumption when bypassing operation is not used.

The addition operation in proposed multiplier is performed by new adder cells if ai is 1 otherwise ICBS is selected by shutting down the proposed adder unit with power gating approach. The new adder architecture as shown in Fig 4.2 has been designed using less hardware components. This adder has lesser area, propagation delay and power requirement than the previously discussed multipliers.

If carry-in is 0, the addition operation is performed by the half adder and sum and carry outputs are selected by multiplexer. The inverted output of half adder cell and or operation of half adder inputs are selected by multiplexer as sum and carry output, if carry-in is 1. Hence, the functionality of full adder cell is obtained using reduced number of transistors in the proposed adder cell.

Consider the test vectors a = 1100 (as multiplicand) (x) b = 1011 (as multiplier) for the proposed multiplier design. The values on the arrow indicate the value of sum and carry bits as shown in Fig 4.4. In (j-1) th row, initial carry is fixed to zero, it replaces the full adder cells with half adder cells as shown in Fig 4.3.

In this row, multiplicand bits a0 and a1 are 0, therefore the vectors (a1b0) and (a2b0) are bypassed to (j)th row by shutting down their respective adder cells with ICBS. In adder cell 3 of (j-1)th row, addition operation is performed by the half adder as the value of multiplicand bit a2 is 1. It generates sum and carry outputs as 1 and 0 respectively and these outputs are passed to the (j) th row adder cell as shown in Fig 4.4. In the next rows, carry input is may be zero or one.

Therefore the logic applied on (j-1)th row is not applicable in succeeding rows. In (j)th row, the carry-in (Ci, j-1) propagating from (j- 1)th controls the addition operation when bypassing scheme is not selected. In this row, a0, a1, and carry-in are 0 for adder cell 1 and adder cell 2, therefore, the bypassing operation is performed with ICBS and sum outputs propagating (j-1)th row are selected by multiplexers at the output.

For adder cell 3 of (j-1)th row, bypassing is not selected and addition operation is performed by proposed adder cell as multiplicand bit a2 is 1. Carry-input of this adder cell is 1 and it will control the addition operation. Therefore, the inverter output and OR operation of half adder inputs are selected as final sum (0) and carry (1) outputs by multiplexer of the proposed adder cell at the output.

Similar operation is repeated in all successive rows of the multiplier. Finally, 10000100 is obtained as output vectors.

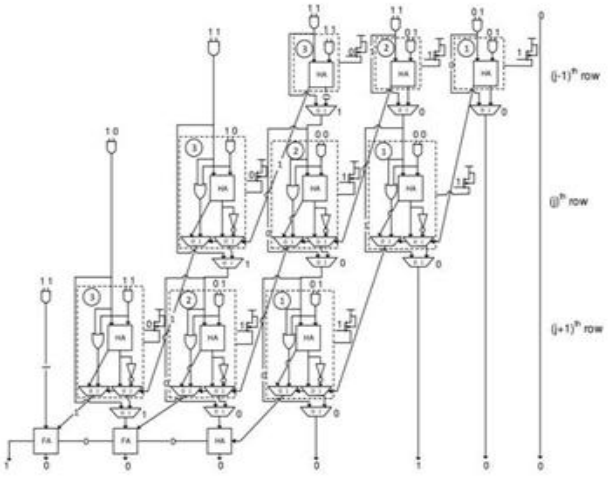

Fig 7. An example of 4 X 4 Modified column bypass multiplier.

II. METHODS AND METHODOLOGY

The proposed multiplier utilizes power gating approach and used PMOS header switch in place of tri state buffer which are used by the previously discussed multipliers. In an active circuit, dynamic power dissipation is the major source of power dissipation where leakage power is less. Dynamic power can be lowered by reducing the switching transitions of the design without affecting its functionality.

Most of the power reduction techniques apply on the multiplier target optimization of parameters involved in equation (1), Logic style and optimized architectures are also used to reduce the power consumption. In case of multiplier, dynamic power can be reduced quarterly by reducing the supply voltage but makes the module sluggish. This further reduces the throughput since the delay is inversely proportional to the supply voltage as shown in eq. (3)

$$Td=(Cload * Vsupply)/(Vsupply - Vth)2 \quad \text{Eq. (4)}$$

Where Vth is threshold voltage of the transistor, Cload is the load capacitance. In the short channel device, the value of Vsupply – Vth is 1.3 in the above equation. It varies according to the technology and assumed to be fixed. In this project, we focus on reducing both dynamic power dissipation and static power dissipation with architecture level and circuit level modifications.

III. WORKING CADENCE

Cadence is an Electronic Design Automation (EDA) environment that integrates various circuit design and verifications applications and tools (both in-house proprietary as well as external third-party vendor tools) in a single framework allowing unified IC design and

verification in a single environment. The tools are generic and allow the designer to conFig the environment depending on the fabrication technology of choice by installing the appropriate PDK.

PDK stands for Process Design Kit. A PDK contains the process technology and needed information to do device-level design in the Cadence DFII environment. When a particular technology is selected, a set of configuration and technology-related files are employed for customizing the Cadence environment. This set of files is commonly referred as a design kit.

GPDK090:

- In this project we are using 90nm Generic Process Design Kit (GPDK090). The GPDK090 has been designed for use within a Cadence software environment.
- GPDK is Generic Process Design Kit. 90 refers to the 90 nm technology which is the minimum channel length of the MOSFETs employed in the given technology.
- Usually, the designs to be fabricated use a PDK which is provided by a foundry for a particular technology (say 180/90/45/22/14 nm). UMC, TSMC, Global Foundries, SCL are some of the foundries. Companies like Samsung, Intel has their own foundries. The PDK provided by any of these foundries will generally be used with the EDA tools provided by vendors like Cadence, Synopsys, and Mentor Graphics to design chips. The GDSII stream file will be sent to the foundries to get the chips manufactured. Along with these EDA tools provided by the EDA vendors, they also provide a Generic PDK which can be used to learn and get familiar with the design flow of the tools.

IV. STEPS FOR SCHEMATIC DESIGN

Step:1 Open the cadence virtuoso software using terminal. Never run Cadence from your root directory, it creates many extra files that will clutter your root. Instead, create a directory or use existing directory other that root (e.g., cadence).

Fig 8. Terminal window.

The command will start Cadence and after a while you should get a window with the "Virtuoso@ 6.1.5", also called Command Interpreter Window (CIW) as below

Fig 9. Cadence virtuoso (CIW) window.

Step:2 Now we need to create a new library (to contain your circuits) so from the Virtuoso (Fig 4.3) Command Interpreter Window (CIW) go to File -> New -> Library from the File menu. You will see a "New Library" window (Fig 5.3).

Fill in the name of the new library (e.g. example) in the dialog window (this will create the library in the directory where you started "Virtuoso", you could also choose to set a path if you wanted another directory). Click on "Attach to existing tech library" and click OK.

Fig 10. New Library Window.

Step-3 In the Virtuoso CIW window go to File -> New -> Cellview. You will get a "Create New file" window (Fig 4.4). Fill in the information in the dialogue window as below and then press OK.

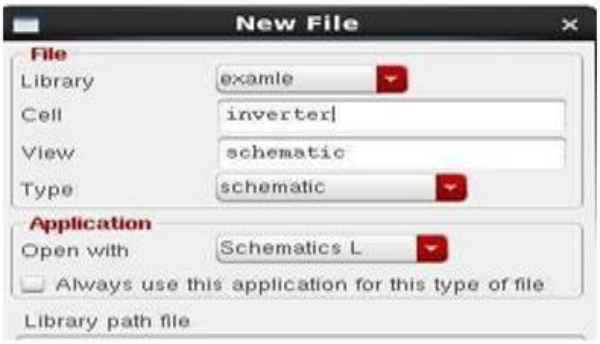

Fig 11. Create New File window.

Wait for a while. "The schematic window will appear. You should get the "Virtuoso Schematic Editing" window as shown below (Fig 4.5)

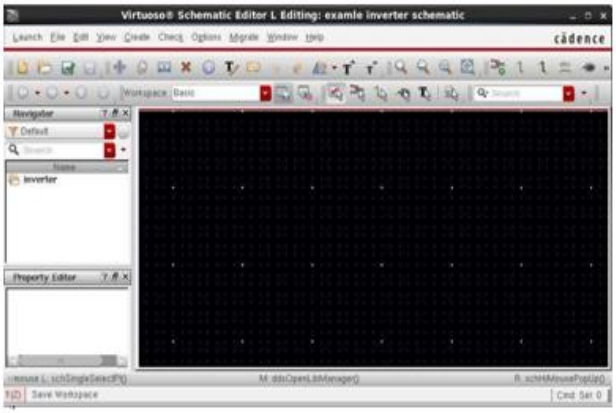

Fig 12. Virtuoso Schematic Editing window.

Step:4 Click on the "Instance" button (icon) on the left side (which looks somewhat like an IC, or click I key) this will pop-up an "Add Instance" window.

Step:5 Now click on the Browse. Another window called "Library Browser – Add Instance" will pop up. We will select all cells we need to design inverter and will place it on the Virtuoso Schematic window. By connecting all cells complete design of inverter.

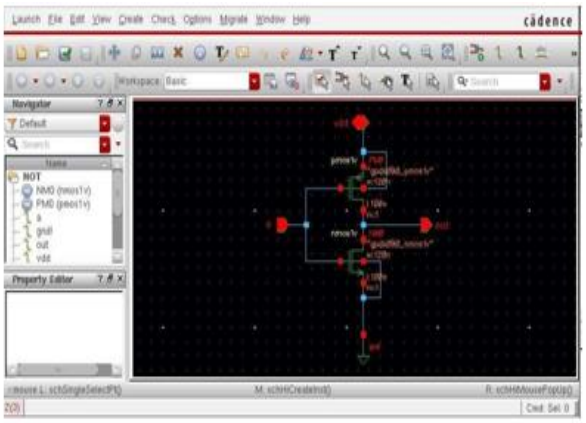

Fig 13. Inverter Schematic.

Step:6 Now you need to Check and Save your design (either click the top left button or go to Design -> Check and Save). Make sure you look at the "Virtuoso" CIW window and see there are no errors or warnings, if there are any you have to go back & fix them!

V. STEPS FOR SYMBOL CREATION

Step:1 In the Inverter schematic window click on Create -> Cellview -> From Cellview. Then Cellview from Cellview form appears. With the Edit Options function active, you can control the appearance of the symbol to generate

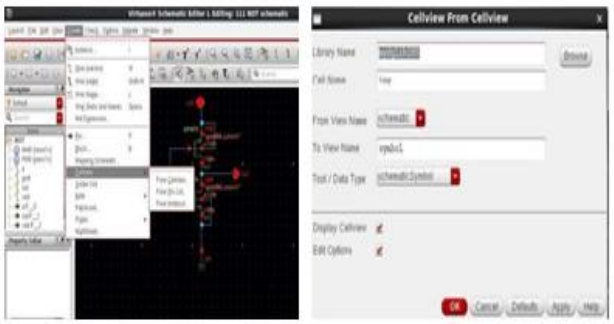

Fig 14. Cellview form window.

Step:2 Click OK in the cellview from cellview. The Symbol Generation window appears. Modify the Pin Specifications as per required symbol.

Step:3 Click OK in the Symbol Generation Options form. A new window displays an automatically created Inverter symbol as shown in fig 4.8

Fig 15. Automatically created symbol.

Step:4 Now edit the shape of symbol as per your requirement, Fig 4.9 shows edited symbol of inverter.

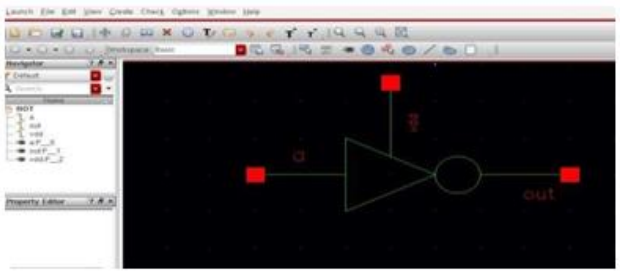

Fig 16. Edited symbol.

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VI. STEPS FOR SIMULATION

Step:1 For simulation of the circuit create new cell view and insert the symbol created before and to set the values for VDD and VSS as shown in fig 4.10

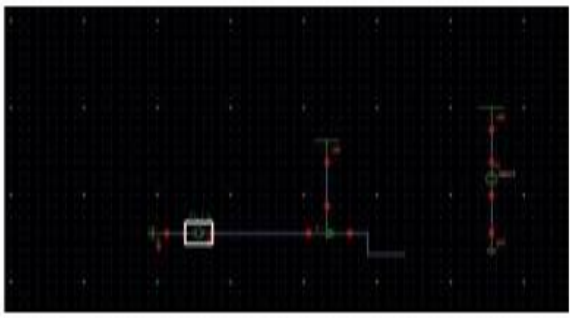

Fig 17. Inverter with inputs connected.

Step:2 In the Virtuoso Schematic window go to Launch -> ADE L Then you will get the simulation window or ADE pop-up window as in Fig. 4.11

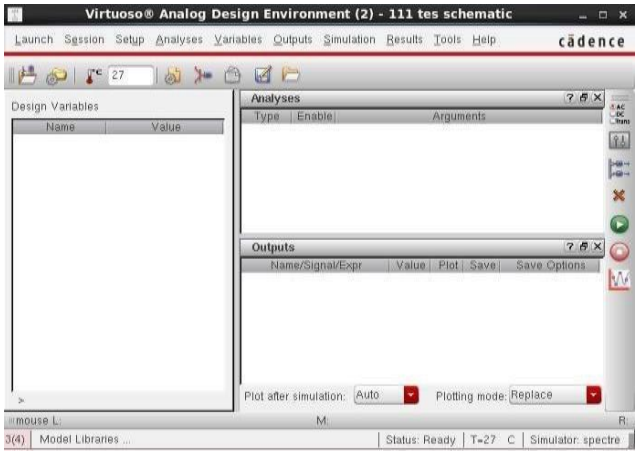

Fig 18. Analog Design Environment window.

Step:3 Now choose the type of simulation. From "Virtuoso Analog Artist" (Fig 4.12) go to Analyses -> Choose. In this case we will choose a transient analysis. Enter the stop time for transient analysis. Let's type 10u for stop time. Click OK.

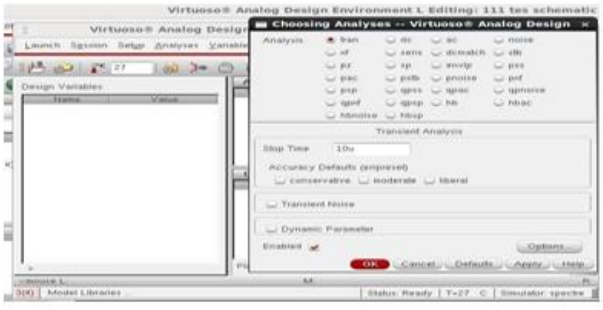

Fig 19. Choosing analysis window.

Step:4 Now in the "Virtuoso Analog Artist" (Fig 5.12) go to "Outputs -> to be plotted -> select on schematic". That will bring your inverter cell view window in front. Select node voltages by clicking on the net. We will click on input and output nets (wires) to select input and output voltages.

Click on the "Netlist and Run Simulation" button (looks like a green light) on the right or go to "Simulation -> Netlist and Run".

It will start simulation. You will need to wait for a while. You should check your "Virtuoso" window for messages while it is running the simulation.

In case you have errors, you will need to go back and correct them. If there are no errors then results window will pop up as shown in fig 4.13

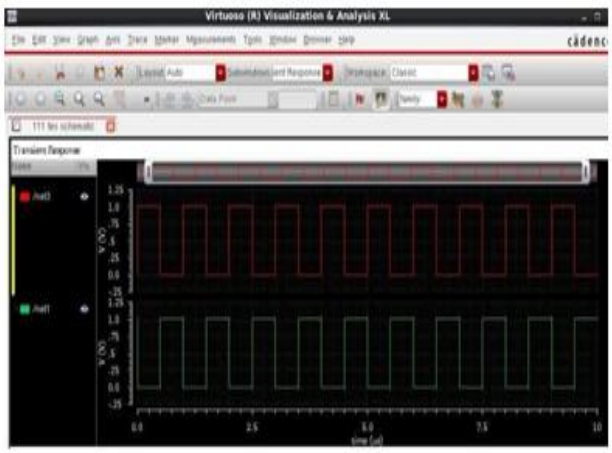

Fig 20. Simulation Results (Transient Analysis).

Power Calculations
There are different methods to calculate power in cadence; this is one of the methods to calculate power.
When the simulation is complete, from the simulator menu choose: Tools->Calculator.

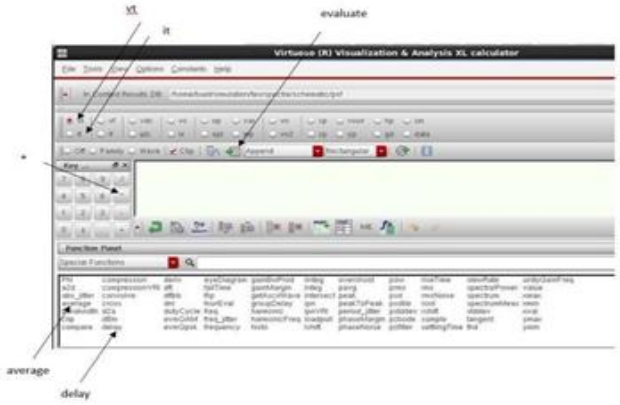

Fig 21. Calculator window.

When the calculator pops up, click on the "vt" button. You will be returned to the schematic, click on the blue wire connecting VDD to its VDC source. The calculator will be populated with: VT("/vdd!"), Meaning 'transient voltage of net vdd!

Next, click on the "it" button. You will be returned to the schematic, click on the top red terminal connecting of the VDC connected to VDD. Then calculator will be populated with: IT("/V1/PLUS"), Meaning 'transient current of the instance V1 (note your source may have a difference instance name, like V2, V3, etc.)

From the calculator pad, click on the * symbol to multiply these two signals together After that under the "Special Functions" category, click on the "average" function You have now built the expression shown in the calculator below.

Fig 22. Power expression.

Press the evaluate button to evaluate the expression. Then the total power should be calculated.

Fig 23. Window showing power.

VII. RESULTS AND ANALYSIS

Performances are compared in terms of power dissipation, worst case delay, power delay product and area overhead. UMC (United Microelectronics Corporation) 90 nm CMOS technology is adopted to implement the proposed multiplier and existing multipliers using cadence virtuoso tool.

Cadence spectre simulator tool is used to estimate the power consumption and worst-case delay. Bypassing, column bypassing and row and column bypassing multipliers. All the multipliers have been designed for 16-bit and 8-bit multiplication operation. The comparison of power consumption at different operating frequencies ranging.

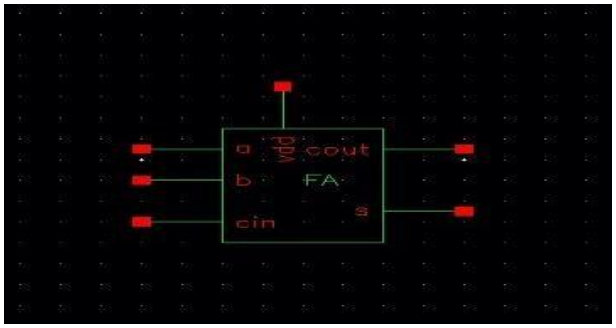

Fig 24. Basic full adder block.

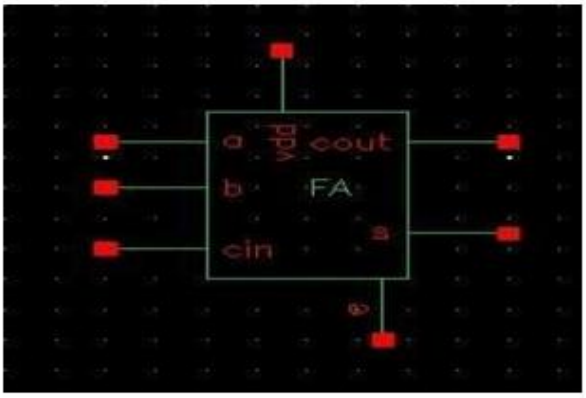

Fig 25. Modified carry save full adder block.

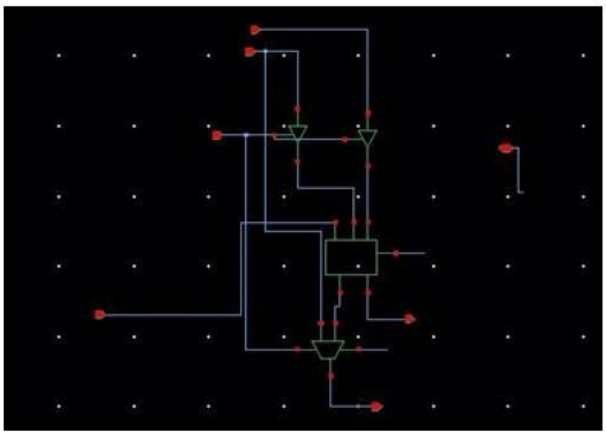

Fig 26. Modified carry save full adder schematic.

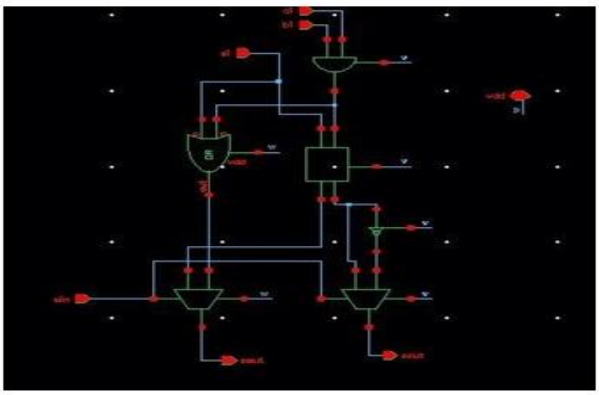

Fig 27. Modified full adder schematic.

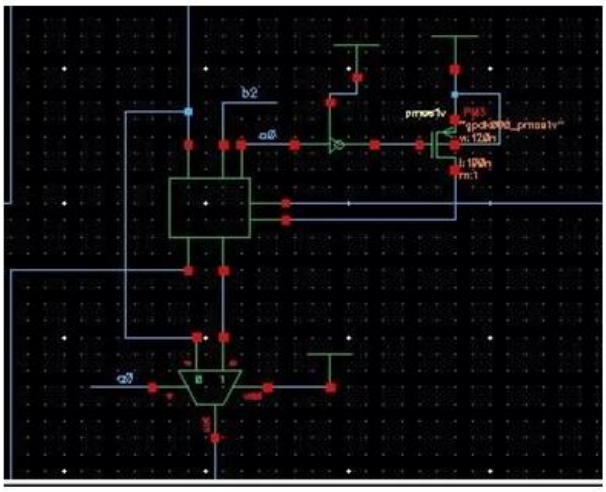

Fig 28. Modified full adder with power gating schematic.

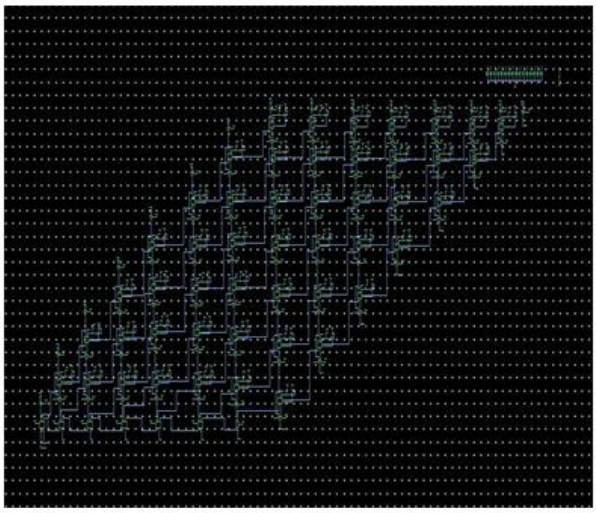

Fig 29. 8 X 8 Modified column bypass multiplier schematic.

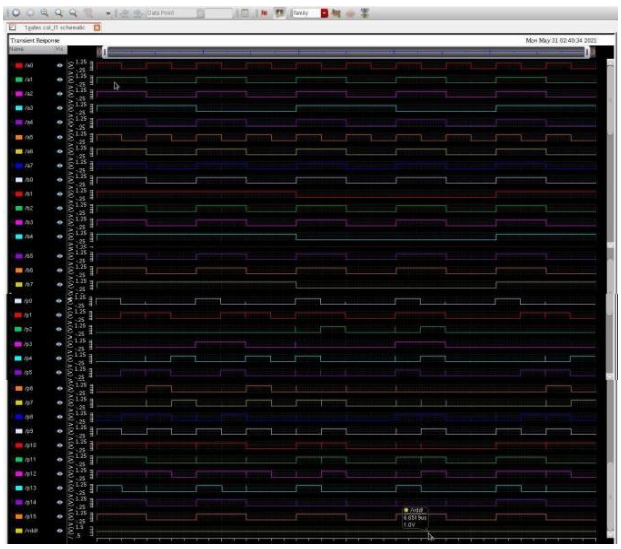

Fig 30. Input and output waveforms of modified Column bypass multiplier.

Table 1. Power Consumption (in µw).

S.NO	Multiplier	1MHz	250 MHz
1	Column bypass	63.83	721.2
2	Modified column bypass	9.393	535.2

Table 2. Power ratio.

S.NO	Multiplier	1MHz	250 MHz
1	Column bypass	5.66	0.979
2	Modified column bypass	0.833	0.726

VIII. CONCLUSION

A low power, high speed proposed multiplier architecture with improved column bypassing scheme has been presented this project. A new adder with optimized hardware is also proposed. The architecture of this adder reduced the power consumption and propagation delay, when ICBS is not in use. Simulation results proves that the proposed multiplier architecture promote reduction of switching transitions and power leakage. It is also found better in terms of area occupancy and propagation delay.

While testing, the input test patterns are taken randomly with an equal occurrence probability of zero's and ones. The proposed multiplier can achieve more power saving if the input test pattern has more no. of zero's than the no. of one's. It has been verified that proposed multiplier outshine previously designed multipliers more effectively at all frequencies and ranks much higher in performance when used for low frequency applications. Therefore, proposed multiplier can be a better choice for assistive listening technology such as hearing aids.

IX. FUTURE SCOPE

The proposed multiplier can achieve more power saving if the input test pattern has more no. of zero's than the no. of 1's. It is difficult to predict which operand having more probability of zero occurrences among multiplier operand & multiplicand operand, to overcome this limitation we can further design multiplier using two-dimensional bypassing technique.

By using two-dimensional bypassing technique, we can have higher power reductions. We can further reduce the multiplier power, delay and area by using modified adders which are designed using techniques like reversible logic gates, m-GDI.

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