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A Review on Designing of Power and Delay Efficient 10T and 14T SRAM Cell

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Abstract- In the last decade, with the advent of smart phones, almost all signal processing devices are becoming the part of a single hardware. From simple calculator to complex image processing, our smart phone contains hundreds of applications which were the part of separate device in the past. This tremendous load of signal processing (addition, subtraction, multiplication, division, numerical integration, convolution, and filtration) eventually loads on the basic computational unit, the full adder. The complex algorithms of today's' mobile applications demand support of very high speed and low power hardware It is necessary to ensure any leakages which cause the read sensing failure and degraded cell stability due to the half-select write. For avoid this situation proposes an equalized bit line scheme to eliminate the leakage dependence on data pattern and thus improves RBL sensing. Also this process a fast local write-back (WB) technique to implement a half-select-free write operation. With hierarchical bit line architecture, it facilitates a local read and a subsequent fast WB action to secure the original data without performance degradation.In the literature survey Non-destructive column-selection-enabled 10T and 14T SRAM for aggressive power reduction, power and delay is presented in brief.

Keywords- Pass Transistor Logic (PTL), LTSpice tools, 10T and 14T SRAM.

I. INTRODUCTION

In CMOS circuits, the main contributions to the power consumption are from short-circuit, leakage, and switching currents. In the following subsections, we introduce them separately.In a static CMOS circuit, there are two complementary networks: p-network (pull-up) and n-network (pull-down). The logic functions for the two networks are complementary. Normally when the input and output state are stable, only one network is turned on and conducts the output either to power supply node or to ground node and the other network is turned off and blocks the current from flowing. Short-circuit current exists during the transitions as one network is turned on and the other network is still active. For example, the input signal to an inverter is switching from 0 to Vdd. It exists a short time interval where the input voltage is larger than Vtn but less than Vdd – |Vtp| .

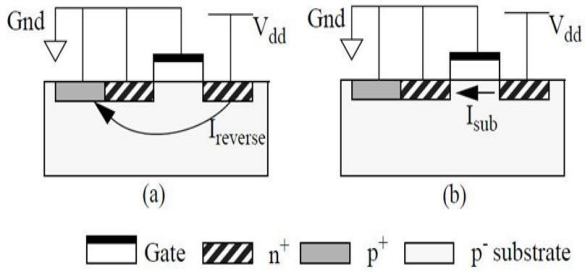

Fig 1. Leakage current types: (a) reverse biased diode current, (b) sub threshold leakage current.

During this time interval, both PMOS-transistor (p-network) and NMOS-transistor (n-network) are turned on and the short-circuit current flows through both kinds of transistors from power supply line to the ground. The exact analysis of the short-circuit current in a simple inverter [6] is complex; it can be studied by simulation using SPICE. It is observed that the short-circuit current is proportional to the slope of input signals, the output loads and the transistor sizes [5]. The short-circuit current consumes typically less than 10% of the total power in a "well-designed" circuit [7].

1. Leakage Power:

There is two contributions to leakage currents: one from the currents that flow through the reverse biased diodes, the other from the currents that flow through transistors that are non-conducting.The leakage currents are proportional to the leakage area and exponential of the threshold voltage. The leakage currents depend on the technology and cannot be modified by the designers except in some logic styles.

The leakage current is in the order of pico-Ampere with current technology but it will increase as the threshold voltage is reduced. In some cases, like large RAMs, the leakage current is one of the main concerns. The leakage current is currently not a severe problem in most digital designs. However, the power consumed by leakage current can be as large as the power consumed by the switching current for 0.06 mm technology.

The usage of multiple threshold voltages can reduce the leakage current in deep-submicron technology.

2. Switching Power:
The switching currents are due to capacitances. The node capacitances interconnection capacitances.

II. POWER AND AREA REDUCTION TECHNIQUES AT CIRCUIT LEVEL

1. Transistor Reordering:
The relative placement of the transistors in the serially connected Metal Oxide Silicon Field Effect Transistor (MOSFET) chain does not alter the functionality of the chain in the circuit. In the complex gates, where group of transistors may be connected in series, flexibility often exists in the relative placement of the transistors. This freedom in transistor placement can be exploited to achieve CMOS circuits with reduced power dissipation. Transistor order in a CMOS gate strongly determines the switching activity, and hence, the power dissipation can be reduced in two ways: by minimizing the drain-source capacitance and by signal probability algorithms to reduce the number of transistors []

2. Transistor Sizing:
Appropriate sizing of transistors in CMOS circuits can be done for minimizing the power consumption under a given delay constraint. Two types of algorithms are available for transistor size optimization: Linear programming and simulated annealing based algorithms satisfy the timing constraint and reduce the size of the gates to reduce the power dissipation.Breadth first algorithm performs an initial power-optimal sizing on each gate. If the power minimal layout satisfies the delay constraint, the process is terminated. Otherwise, the power-delay optimal sizing is continued to reduce size of transistors on the critical paths until the timing target is met.

An algorithm of this type is proposed by [2][3] This algorithm is more complex than the previous ones because it takes into account not only the power dissipation which is due to the charging of the circuit capacitance but also the short circuit power dissipation. Another interesting conclusion by [4]is that the active area is not a reliable indicator of power consumption of the circuit. It is shown that the power consumption of a CMOS circuit is a convex function of an active area. The objective of minimizing the power dissipation for a transistor sizing algorithm is different from that of minimizing the active area.

3. Path Balancing:
In order to reduce the glitching activity in a circuit, the delay of all true paths that converge at each gate must be roughly balanced, because path balancing leads to nearly simultaneous switching on the various gate inputs and the possible hazards at the output of the gate are eliminated as shown in Figure 4. This in turn reduces the average power dissipation in the circuit. Path balancing can be achieved before or after technology mapping. Before technology mapping it is achieved by logic decomposition or selective collapsing. After technology mapping it is achieved by delay insertion and pin reordering.

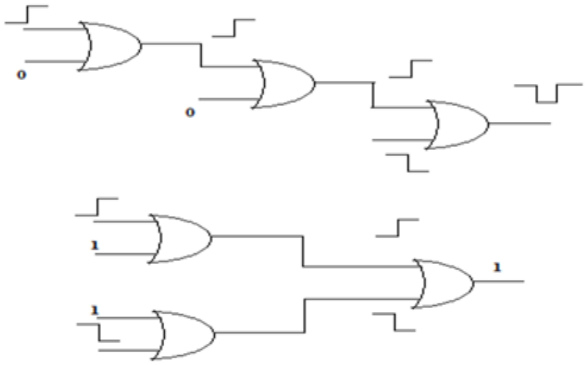

Fig 2. Example illustrating the effect of path balancing.

The idea behind selective collapsing is that, by collapsing the fan-ins of a node, the arrival timing the output of that node can be changed. Logic decomposition leads to minimization of the level difference between the inputs of the nodes that are driving high capacitive nodes. The delay insertion procedure tries to balance the delays of all paths in the circuit. The key issue in delay insertion is to use the minimum number of delay elements to achieve maximum reduction in spurious switching activity.

Finally, pin assignments can be changed to balance path delays. This is possible because the delay characteristics of CMOS gates vary as a function of the input pin that is causing a transition at the output.The idea behind selective collapsing is that, by collapsing the fan-ins of a node, the arrival time the output of that node can be changed. Logic decomposition leads to minimization of the level difference between the inputs of the nodes that are driving high capacitive nodes. The delay insertion procedure tries to balance the delays of all paths in the circuit.The key issue in delay insertion is to use the minimum number of delay elements to achieve maximum reduction in spurious switching activity.

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4. Voltage Scaling and Multiple Supply Voltage:
Scaling of voltage levels will be an important issue in the design of future digital systems. The main driving forces are the desire to produce complex, high performance systems on a chip. It is projected that the various ASICs and memory elements will also switch to reduced supply voltages to meet stringent power constraints. One of the main problems in this approach is the availability of the complete chip set to make up systems at reduced supply

voltages. This problem is overcome to some extent by mixing and matching different supply voltages on the chip. Clocking-In many synchronous applications, a significant amount of power is dissipated by the clock. Generally this is the only signal that switches all the time and it usually has to drive a very large clock tree.

Moreover, in many cases the switching of the clock causes a lot of unnecessary switching activity. Consequently, recent circuits are designed with controllable clocks. In other words, from the master clock, other clocks are derived that can be slowed down or stopped completely with respect to the master clock under certain conditions. The circuit is therefore partitioned into small blocks that have their own derived clocks.

The power savings achieved in this manner are application dependent.In addition significant power savings are achieved by stopping the clock fed in the idle modules. Sections of the clock tree are turned ON or OFF by gating the clock signal during the active or idle mode by associating every node in the clock tree with a binary string of 1s or 0s representing the active/idle status of the node in that time slot.

5. Circuit Styles:
Typically a given logic function can be realized using many different logic styles such as static CMOS, dynamic CMOS, pass transistor, differential cascade switch voltage logic, etc. Among these, the pass transistor logic style is the most suitable for low power design, because the pass transistor logic can be designed with fewer transistors when compared with conventional static CMOS. For example, the circuit of a static CMOS full adder requires 40 transistors, whereas a circuit designed using pass transistor logic requires only 28 transistors. Researchers have therefore explored various pass transistor logic styles such as Complementary Pass transistor Logic (CPL), Swing-Restored Pass transistor Logic (SRPL), and Differential Cascade Voltage Switch with Pass transistor Gate (DCVSPG).[1]

A CPL design uses NMOS pass transistors and therefore a high level drop at the output. CMOS inverters are connected at the output stage to compensate for the dropped signal level as well as to increase the output driving capability. Although the output voltage is restored, the lower high level increases the leakage current in the CMOS inverters. In order to avoid this, cross coupled PMOS loads are added to recover the high level and enlarge the operation margin. Typically, small PMOS transistors are used to prevent degradation in switching speed. The DCVS style is a slight variation of the CPL style and uses NMOS pass transistor logic with cross coupled PMOS loads.An SRPL design uses NMOS pass transistor logic coupled with a CMOS latch. Since the CMOS latch flips in a push-pull manner, it exhibits greater operating margin, less static current and faster compared to cross-coupled CMOS loads. This approach is ideal for circuits with small load capacitance. Moreover, these circuits are more robust against process variations.

6. Folding:
In synthesizing DSP architectures, it is important to minimize the silicon area of the integrated circuits, which is achieved by reducing the number of functional units (such as adders and multipliers), registers, multiplexers, and interconnection wires. The folding transformation is used to systematically determine the control circuits in DSP architectures, where multiple operations (such as addition) are multiplexed to a single functional unit (such as pipelined adder). By executing multiple algorithm operations on a single functional unit, the number of functional units in the implementation is reduced resulting in an integrated circuit with low silicon area.[2]

III. LITERATURE SURVEY

Digital signal processors and ASICs rely on the efficient implementation of arithmetic circuits to execute dedicated algorithms such as convolution; correlation and digital filtering (Chang et al 2005).The execution of these algorithms require dedicated ALU and MAC architectures. Adders, multipliers and counters are the key elements of these arithmetic units and this chapter discusses the various algorithms and architectures proposed in the design of these key elements.[3]

Aaina Nandal et.al (2018) in this paper ECRL with sleepy keeper technique has been presented. The proposed adder shows less power dissipation and less power delay product (PDP). The circuits have been simulated in 0.18µm CMOS technology using Mentor Graphics. The proposed Full adder indicates power dissipation of 129.819pW with a delay of 135.97ns at supply voltage of 1.8V. Simulations have been completed with different supply voltages [1.0-1.8] V. Power dissipation of proposed full adder circuit have been contrasted with earlier reported full adder designed circuits and proposed approach indicates better outcomes.

S Lakshmi et.al (2018) in this paper a novel 1 bit energy efficient hybrid adder has been introduced which can optimize performance parameters like power and delay of two CMOS hybrid full adder circuits described in this paper. The first described design is implemented with normal Complementary metal oxide semiconductor (CMOS) and second design is a hybrid model of CMOS and transmission gate logic (CMOS-TGL).

The proposed model is hybridized with Complementary metal oxide semiconductor, pass transistor and modified gate diffusion input logics (CMOS-PT-MGDI) together to ensure low power and high speed. The performance parameters such as power, delay and area of 1 bit full adders was analyzed and tabulated.

All the circuits were implemented using cadence virtuoso tool in 90nm technology for 1.2V supply.

Gautam Nayan et.al (2019) Addition is a standout amongst the most fundamental operations in VLSI frameworks such as microprocessors and digital signal processing systems. Therefore, the adders must render a high speed operation into existence. This paper proposes a novel implementation of 8-bit adder architecture using modified Gate Diffusion Input (m-GDI) approach. The primary blocks of adder are partial full adder, 1-bit full adder, 4-bit ripple carry adder (RCA), 4-bit carry look ahead adder (CLA). The proposed adder architecture devours 70% lesser area, 71 % lesser delay and 35% lesser power dissipation w.r.t traditional CMOS design. The proposed adder is implemented utilizing Cadence Virtuoso Tool in 180nm technology.

Somashekhar Malipatil et.al (2020) GDI (Gate Diffusion Input) is a new technique of low power digital circuit design is proposed. This technique allows minimization of area and power consumption of digital circuits. In this design XOR gate is designed using 3 transistors and CMOS full adder is designed based on two 3T XOR and one 2T Mux. Using 8 transistors the full adder is designed in this paper and voltage scaling also done by reducing supply voltage. In this proposed full adder, the power consumption 4.604μW is achieved and the total area is 144μm 2.

M. Keerthana et.al (2020) Adders is plays a vital role in digital and VLSI systems. Arithmetic operations are an essential part of digital systems. During VLSI systems, the entire research is on lowering the scale of transistors for enforcing any other digital system. This proposed architecture implemented by different types of logic systems; each logic performs the different role in the hybrid system. The hybrid Full Adder cell with one bit is implemented in this structure.

The proposed method is investigated using 22-nm CMOS hybrid full adder. The proposed architecture demonstrates substantial efficiency in power consumption and delay, based on simulation results. The simulation result expressed that the full adder circuit is used to modern high speed central processing unit in the data path architecture. This form of hybrid Full Adder, reduces the delay and increasing efficiency and mainly used in nano technology applications. The average power consumption of 1.1055 μW with moderately low delay of 7.0415ps was found to be extremely low for 0.8-V supply at 22-nm technology. This kind of adder allocates significant improvements in power, high speed and area compared with previous full adder designs.

Boopathy. E Veera et.al (2018) Using multioutput domino CMOS logic, a cost effective implementation of Manchester carry chain (MCC) adder for 8-bit is designed in this paper. From this adder carries are generated parallels employing two main carry chains of 4-bit. The suggested 8-bit adder module comprises confined length of carry chain. As a result of this ability, it is applied to realize broader adders and as well it guides to betterments in functioning rate equated to the related adders established upon the classical 4-bit MCC adder module.

A. Sedhumadhavan et.al (2020) In this work, the speed and power performance of static and dynamic circuits technology based reverse carry propagate full adder (RCPFA) have been studied with the help of SPICE tools. The main feature of RCPFA is that the carry signal propagates from MSB (Most-significant-Bit) to LSB (least-significant-Bit). Therefore, in RCPFA circuits the input carry signal has very high importance than the output carry signal. The RCPFA circuits were designed using 22 nm CMOS strained silicon technology with a power supply of 0.8 volt. Finally the influence of operating temperature on the speed and power performance of RCPFA adders also been studied. Simulation results show that dynamic RCPFA circuits out performs the static RCPFA circuits in terms of speed and power.

Zarin Tabassum et.al (2018) This paper analyzes & compares four adders with different logic styles (Conventional, transmission gate, 14 transistors & GDI based technique) for transistor count, power dissipation, delay and power delay product. It is performed in virtuoso platform, using Cadence tool with available GPDK - 90nm kit. The width of NMOS and PMOS is set at 120nm and 240nm respectively. Transmission gate full adder has sheer advantage of high speed but consumes more power.

GDI full adder gives reduced voltage swing not being able to pass logic 1 and logic 0 completely showing degraded output. Transmission gate full adder shows better performance in terms of delay (0.417530 ns), whereas 14T full adder shows better performance in terms of all three aspects.

Chang Chin Kai et.al (2020) Fault-tolerant architecture plays a crucial role in the safety and mission-critical application such as space and medical application. These applications require high reliability to maintain continuous operation without fault. The tremendous increase in the integration density and the downscaling of the nanotechnology cause the system exposed to the soft error more frequently. This project concerns the development of a 16-bit fault tolerant sparse Kogge Stone Adder (KSA) by implementing Triple Modular Redundancy (TMR) approach. The results show that the fault tolerability had been greatly improved at almost double the masking rate of the adder alone and can be operated at the maximum frequency of 166.67 MHz. Application-Specific Integrated Circuit (ASIC) implementation using Silterra 0.18 μm CMOS technology is conducted using Synopsys Electronic Design Automation tools.

IV. MOTIVATION FOR THE RESEARCH

Large integration of data path elements in processing architectures used for portable applications reduces residual energy of battery quickly. Dynamic power dissipation is the significant contributor to the total power consumption of a digital CMOS circuit. The technology scaling reduces dynamic power dissipation to a significant amount at the expense of leakage power dissipation. The dynamic power can be reduced by reducing the supply voltage at the expense of high delay. So the research is focused on reducing dynamic power dissipation and minimizing critical delay by circuit level changes.

Leakage power dissipation is directly proportional to the area of the CMOS circuits; the focus of the research also concentrates on reducing gate count of CMOS arithmetic circuits. The thesis focuses on power and area reduction of data path elements used in processing architectures and due consideration is given for delay minimization. The elements considered are adders, multipliers and counter circuits. The following types of circuits are proposed and their implementation in processing applications is analyzed in this research.

Adders-Full Adder (FA) is the most widely used adder circuits in processing architectures and decimal adder is the important component of ALUs designed for business and commercial applications. They are the key elements as they lie in the critical path and determine the overall performance of the system. Careful design of these adders is required to reduce delay and power dissipation of processing architecture. FA designs using single logic style for both sum and carry have certain limitations. FA using complementary pass logic suffers from threshold voltage drop problem and FA using CMOS transistors and transmission gates have poor driving capability. Recently hybrid FA using Branch Based Logic (BBL) for carry.

V. SYSTEM LEVEL DESIGN

A system typically consists of both hardware and software components, which affect the power consumption. the charging and discharging of node mainly include gate, overlapping, and The system design includes the hardware/software partitioning, hardware platform selection (application-specific or general purpose processors), resource sharing (scheduling) strategy, etc. The system design usually has the largest impact on the power consumption and hence the low power techniques applied at this level have the most potential for power reduction.

At the system level, it is hard to find the best solution for low power in the large design space and there is a shortage of accurate power analysis tools at this level. However, if, for example, the instruction-level power models for a given processor are available, software power optimization can be performed [59]. It is observed that faster code and frequently usage of cache are most likely to reduce the power consumption. The order of instructions also have an impact on the internal switching within processors and hence on the power consumption. The power-down and clock gating are two of the most used low power techniques at system level. The non-active hardware units are shut down to save the power. The clock driver, which often consumes 30-40% of the total power consumption, can be gated to reduce the switching activities as illustrated in Fig. 3.

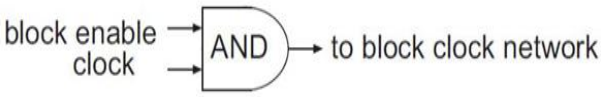

Fig 3. Clock gating.

The power-down can be extended to the whole system. This is called sleep mode and widely used in low power processors. The Strong ARM SA-1100 processor has three power states and the average power varies for each state [60]. These power states can be utilized by the software through advanced configuration and power management interface (ACPI). In the recent year, the power management has gained a lot attention in operating system design. For example, the Microsoft desktop operating system supports advanced power management (APM). [4][5]

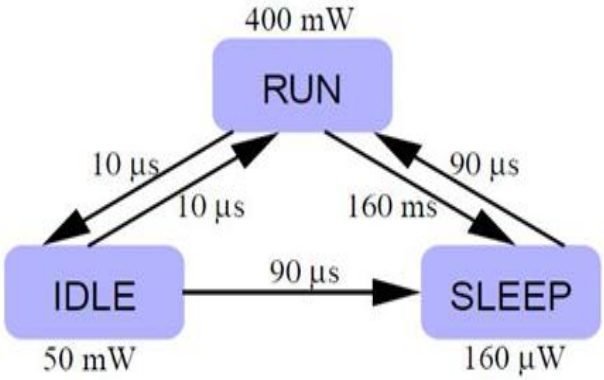

Fig 4. Power states for Strong ARM SA-1100 processor.

The system is designed for the peak performance. However, the computation requirement is time varying. Adapting clocking frequency and/or dynamic voltage scaling to match the performance constraints is another low power technique.

The lower requirement for performance at certain time interval can be used to reduce the power supply voltage. This requires either feedback mechanism (load monitoring and voltage control) or predetermined timing to activate the voltage down-scaling. Another less explored domain for low power design is using asynchronous design techniques.

The asynchronous designs have many attractive features, like non- global clocking, automatic power down, no spurious transitions, and low peak current, etc. It is easy to reduce the power consumption further by combining the asynchronous design technique with other low power techniques, for instance, dynamic voltage scaling technique [6]. This is illustrated in Fig. 5.

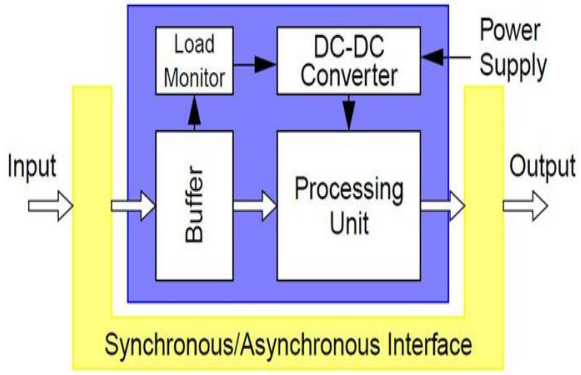

Fig 5. Asynchronous designs with dynamic voltage scaling.

Algorithm Level:
The algorithm selection has large impact on the power consumption. For example, using fast Fourier transform instead of direct computation of the DFT reduces the number of operations with a factor of 102.4 for a 1024-point Fourier transform and the power consumption is likely to be reduced with a similar factor. The task of algorithm design is to select the most energy efficient algorithm that just satisfies the constraints. The cost of an algorithm includes the computation part and the communication/storage part.

The complexity measurement for an algorithm includes the number of operations and the cost of communication/ storage. Reduction of the number of operations, cost per operation, and long distance communications are key issues to algorithm selection. One important technique for low power of the algorithmic level is algorithmic transformations [7] regularity, and locality of an algorithm. Reducing the complexity of an algorithm reduces the number of operations and hence the power consumption.

The possibility of increasing concurrency in an algorithm allows the use of other techniques, e.g., voltage scaling, to reduce the power consumption. The regularity and locality of an algorithm affects the controls and communications in the hardware.

The loop unrolling technique [8] is a transformation that aims to enhance the speed. This technique can be used for reducing the power consumption. With loop unrolling, the critical path can be reduced and hence voltage scaling can be applied to reduce the power consumption. In Fig. 3.6, the unrolling reduces the critical path and gives a voltage reduction of 26% [9]. This reduces the power consumption with 20% even the capacitance load is increases with 50% [10]. Furthermore, this technique can be combining with other techniques at architectural level, for instance, pipeline and interleaving, to save more power.

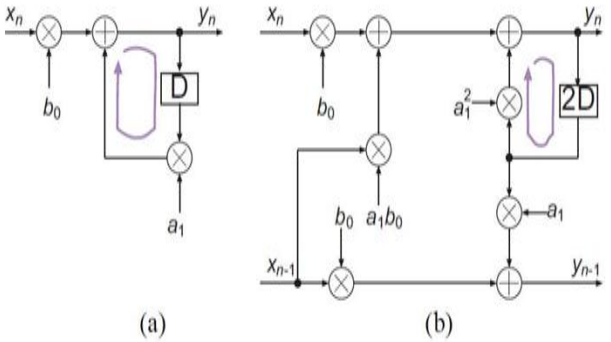

Fig 6. (a) Original signal flow graph. (b) Unrolled signal flow graph.

In some cases, like wave digital filters, the faster algorithms, combined with voltage-scaling, can be chosen for energy-efficient applications [11].

2. Circuit Level:
At the circuit level, the potentials power saving are often less than that of higher abstract levels. However, this cannot be ignored. The power savings can be significant as the basic cells are frequently used. A few percents improvement for D flip-flop can significantly reduce the power consumption in deep pipelined systems. In CMOS circuits, the dynamic power consumption is caused by the transitions. Spurious transitions typically consume between 10% and 40% of the switching activity power in the typical combinational logic .In some cases, like array multipliers, the amount of spurious transitions is large. To reduce the spurious transitions, the delays of signals from registers that converge at a gate should be roughly equal. This can be done by insertions of buffers and device sizing [12].

The insertions of buffer increase the total load capacitance but can still reduce the spurious transitions. This technique is called path balancing.Many logic gates have inputs that are logically equivalent, i.e., the swapping of inputs does not modify the logic function of the gate. Example gates are NANDs, NORs, XORs, etc. However, from the power consumption point of view, the order of inputs does effect the power consumption. For instance, the A-input, which is near the output in a two-input NAND gate, consumes less power than the B-input closed to the ground with the same switching activity factor. Pin ordering is to assign more frequently switching to input pin that consumes less power. In this way, the power consumption will be reduced without cost. However, the statisticsof switching activity factors for different pins must be known in

advanced and this limits the use of pin ordering [13][14[15].

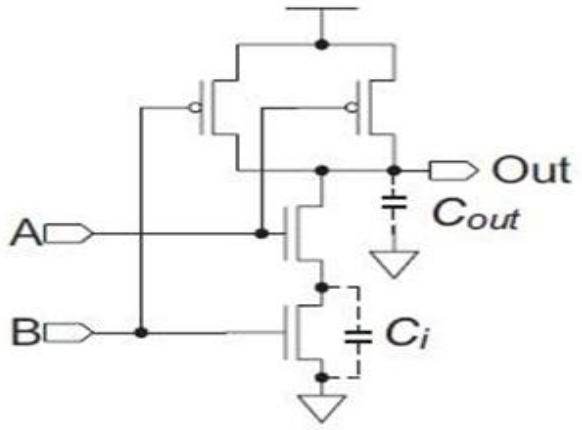

Fig 7. NAND gate.

VI. CONCLUSION

In this paper, various one bit full adder cells design has been reviewed from the most recent published research work. The comparison of full adder cells with each other in term of power, delay, operating frequency and transistor count is done. Based on survey, it is conclude that the new 14T and 10T have good signal level, consume less power and have high speed compare to all other designs at low supply voltage. This circuit is suitable for arithmetic circuits and other VLSI applications with very low power consumption and very high speed performance this paper present an analysis of popular 1-bit full adder circuits.

The analysis metrics comprised of power, delay, power-delay-product, area, and threshold loss. As an important unit of various hardware computational blocks, the transistorlevel design of the full adder circuit has been evolving for decades. In this comparative study, we focus on the highly cited designs of last two decades. This paper serves as a quick reference for the VLSI designers and researchers in selecting appropriate circuit for the computational block and further improvement, respectively.

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