International Journal of Scientific Research & Engineering Trends
Volume 8, Issue 1, Jan-Feb-2022, ISSN (Online): 2395-566X

Control Strategy of Diode Clamped 3 Level Inverter With PV System as Separate DC Source

Mantu Kumar, Devbrat Kumar, Manish Kumar
Department of Power Electronics
MIT ,Bhopal,MP,India

Abstract-In the recent year, every day utility has been increased which causes the increase in power demand. In case of conventional power sources, they are using fossil fuels and other resources, which contribute to fly ashes, CO2 gas emissions, which cause global warming. These resources will be affected by the negative impact of the alternation of alternating shale. Recently India is facing coal shortage. To improve and reduce the dependency of the crisis of fossil fuels, researchers has come up with an interest in research to usage of non-conventional sources. In the last few decades non-conventional energy sources became a great alternative of conventional sources like fossils fuels, and researchers has focused on latest energy production alternatives like solar, wind, hydel and geothermal energy sources and continuously developing ecological environment for creating new sustainable natural resources.In fact, the power transmission system is the source of power supply in AC and all loads (appliances / machinery). Most of them need A.C power from source as an important source of their energy. The main requirement of energy is in form of AC, so we use Inverter as conversion instrument (DC to AC). Basic inverters are facilitated and limited up to 2- level only. Due to efficient and bulky requirement by industrial supply,2-level inverters are unable to full-fill the requirement. Due to the efficiency and such limitations of 2-level inverter, huge power inverter (multi-level) are used which are capable for providing high energy at high efficiency loads to and also repeal the limitations of basic 2-level inverter. Multilevel inverter uses n levels to provide effective and efficient power quality and power demands, very less losses at time of switching (since they uses electronic element), very high voltages stability, a wide voltage control range rather than conventional 2-level inverter. It also provide power at reduced harmonics. The main trump card of using multi-level inverters (MLI) is "it produces less harmonics disturbance and also reduces losses due to switching at time of operations". Multi-level inverters are able to handle high power load in comparision to 2-level inverter with guaranteed no affect on the output of multi-level voltages. Multi-level topologies are available in wide range, but the well-knownand widely used are of following types: - 1. Cascade H-bridge Multi level Inverter (CHMI):- • It utilises series connections ofan N-bridges (multilevel) inverters. 2. Diode Clamped Multilevel inverter (DCMI):- • It uses an [2*{N-1}] semi-conductor switches for n-level inverter circuit. • It also uses a series connection of capacitor parallel to the dc bus which is clamped bythe diode. 3. Flying Capacitor Multilevel Inverter (FCMI):- • Capacitor is usedinstead of clamping Diode. NOTE:- Multi-level inverters uses many numbers of semi-conductor switches which is disadvantage of the multi-level inverters over 2 level inverter.

Keywords-Multi-level Inverter, Dual Clamped Inverter, Flying Back Inverter, Control Scheme, Harmonic Injection, SPWM Method, PV Array.

I. INTRODUCTION

1. Why we useDCMI inverter ?
The output voltage can be determined by using following:-

- Clamping diode
- Cascaded-capacitor in diode clamped multi-level inverter (DCMI).

To do the topology of the inverter we use topology in three levels or in five levels. The 3-statetopogrphy is regarded as NPC inverter and it has numerousreach in several app in case of high-power, medium-voltage drives (HPMV). NPC inverter is mainly used forreducing dv/dtand total harmonic distortion (THD) in its ac output voltage incomparision to conventional 2-level inverters. The inverter which are used as medium level drive to finda suitable voltage level without switching device in-series combination, which is regarded as the main feature of the device. The input provided is dc in nature which is splited between two capacitor, and a floating neutral terminal is provided. The diodeswhich are connected to floating terminals are called as the clamping diode.

Since the industry is growing very rapidly and also require very efficient and high power, so we need such equipment which can be operated and handle these high power demandalso which can provide the power demand in the megawatt (MW) level. Such operations are very difficult to obtain from single power conventional switchesand connect it directly to medium voltage grids about 66Kv. To overcome such problems new class of multi-level inverters was introduced in the power sector as aalternative, to handle such medium and high power applications.

In the initial phase of research of high power switching three level switches were invented. Afterwards not only 5-level but also n-level switches were invented as cure of such high-power applications. By using n-level switches, n-multi-levels voltages are found at output.

II. MULTILEVEL INVERTERS

In modern days every electrical equipments works on ac source, but in case of dc input we require inverter to convert dc to ac. For example solar powered car or battery driven cars the dc input to ac. The signal obtained at output is variable in nature (both magnitude and frequency). Filters are used at yield to eradicate higher order harmonics and make the signal at output terminalsmooth.

In normal conditions the batteries are charged by dc which is converted from ac using transformer and rectifiers. And when the power went off the battery provides power to the ac appliances which is converted through inverter.Here the classification of inverters is given which are familiarized in the power electronics family.

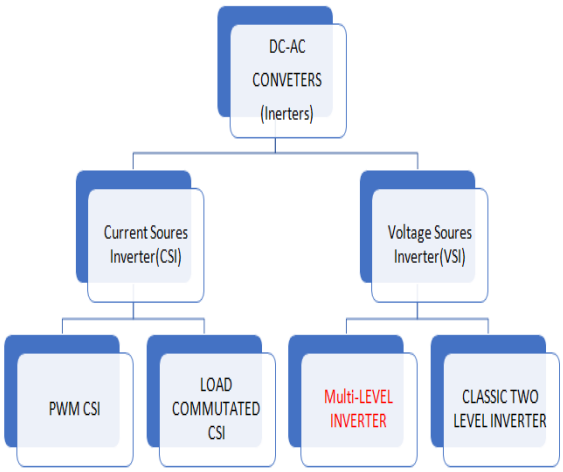


Fig 1. Types of inverters**.**

- High power can be converted form medium VSI using MLI. The MLI can convert high power from medium VSI.
- By using MLI we can generate high power from low rating.
- Different PWM techniques are used for changing the frequency.

1. Working principle of Multilevel Inverters:

The two level inverter is the most simplest and familiar type inverter which can generate ac voltage to dc. Dual stage inverter can engender two unlike voltage levels. For example if we provide V as input signal the output will be +V/2 and –V/2

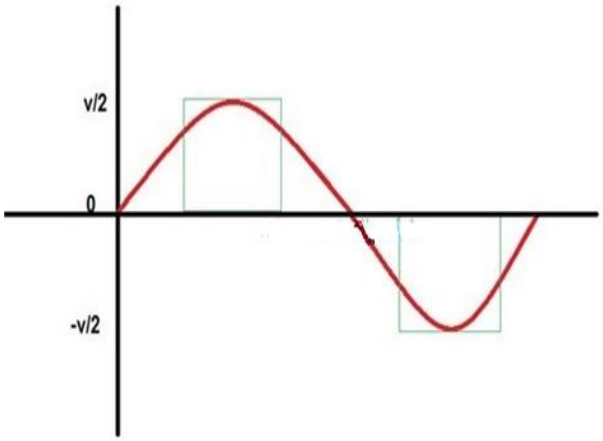


Fig 2.Output of inverter.

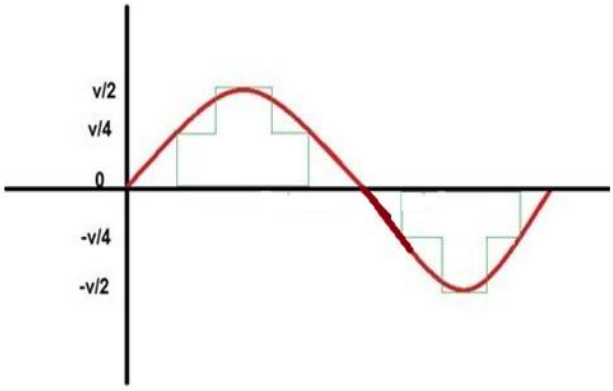


Fig 3.Output of inverter.

In this process of voltage conversion there is some restriction and it seeds some abnormality in the output voltage. Due to abnormal output it is not suitable for every application though this technique works properly in few applications. The technological progress of Multi-level inverter is the effort to reduce the noise of the output wave form and it the modified version of two-level inverter. In MLI the output wave form is smoother than 2-level inverter and it is created by adding of more than two levels. The higher the voltage level, the alteration is minimum.

2. Types of Multilevel Inverters:

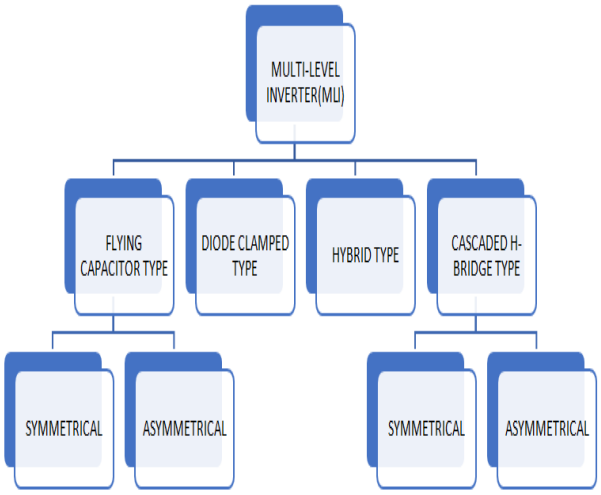


Fig 4. Types of multilevel inverter.

The Multilevel inverters are classified in according to their switching technique and the type of available source to the inverter.in the fig.3 the classification is shown:

- CHMLI
- DCMLI
- FCMLI

III. TOPOLOGY OF N-LEVEL INVERTER

1. Cascaded H-Bridges:
The fig.1.circuit diagram ofH-bridge, inverter. Different voltage levels are found by triggering withes
S1, S2
S3 and S4.

By proper operation of switches three voltage levels are found which are–Vdc, 0, +Vdc.

Operation of switches:-
S1 and S4 are turned on
Output=+Vdc,
S2 and S3 are turned
Output=–Vdc
S1,S2,S3, and S4 are turned on
Output=0

The output of the all n-multi-level inverters are obtained in form of summation of due to each individual. The output which are addition to n-multi-level inverter are determined as

n = (2s+1)

s = number of SDCS.

Let's assume 13-levels cascaded H-bridge inverter having 5 unique dc source and 5 full-bridgethat areas shown in Fig.2.1.

$V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5}$.

Theforier-transform obtained by step wave-form is givenin fig.2.2 is

$$H(n)=\frac{4}{\pi n}\left[\cos(n\theta_1)+\cos(n\theta_2)+...+\cos(n\theta_s)\right], \quad \text{where } n=1,3,5,7,... \qquad .....3.1$$

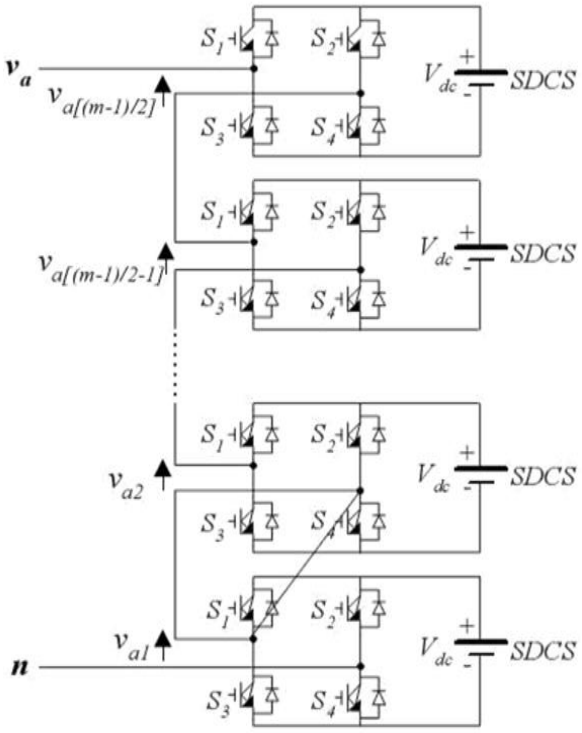


Fig 5. Single-phase circuit of a multilevel cascaded H-bridges inverter.

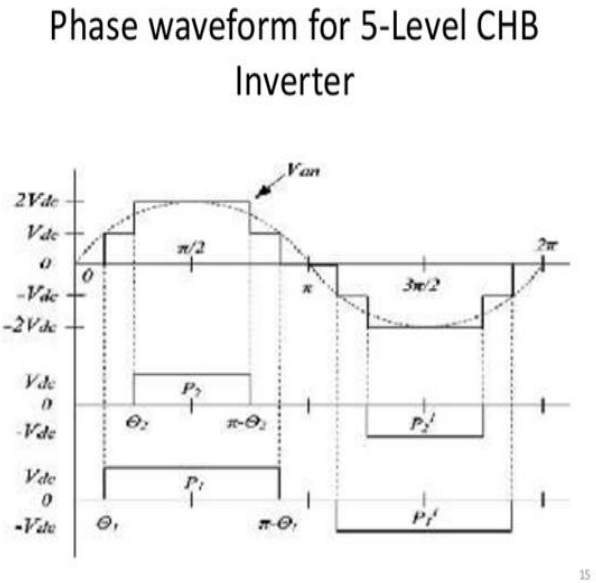


Fig 6.**Phase waveform of 5-level inverter.**

To eliminate the total harmonic distortion (THD), conducting angles are chosen accordingly byappropriate

manner. By the help of changing conducting angles the shapes of obtained stepped waves can be changed.

The lower order odd harmonics (2n□1) th are eliminated by proper operation of selecting conduction angle.A model was described that consists of llr reactor with the electrical system which can either provide or absorb reactive power in form of current from an electrical system.

For renewable energy sources cascade system are considered as ideal connection, since it required separate dc sources (SDCS), which are used in connection such as PV cells or fuel cells. Series inverters are utilized formain traction drive in e-traction, whereasmultiplebatteryare provided as SDCS. Sometimes ultra-capacitors are very useful for the purpose of SDCSs.

The cascaded inverter serves as either as rectifier or as a charger for the bank of battariesused in electric tractionwhile the electric commutes are connected to an acsupplyshown in Fig 2.3.0 additionally; they are used for regenerative modes.

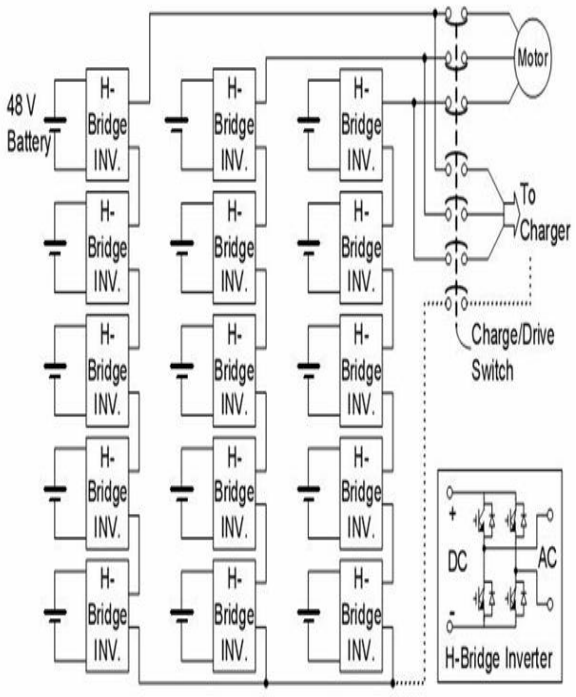


Fig 7.CHB Inverter Model.

1.1Pros:
The total no. of output voltage are nearly double the no. of inputs

(m = 2s+1)

This level of output enhances the manufacturing process and makes itquick, reliable and cheap.

1.2Cons:

There is requirement of SDCS source for each of the H-bridges separately. This will make the circuit "more-composite and sizeable".

A different kind of cascaded multi-level (n-level) converter with x-mers using standard 3-□dual-level converters has been proposed. The circuit is shown in Fig.6

The different voltages obtained from converters are addedby use of transformer, by using it in proper manner. For proper summation of voltages obtained from three different converters, the output voltage of the converters must be synchronized with phase difference of 120□.

The synchronized output voltage obtained from transformer output can be represented mathematically in form of expression:-

$$V_{ab} = V_{a1\text{-}b1} + V_{b1\text{-}a2} + V_{a2\text{-}b2}$$

X-mers are used for providing boost in unlike voltage. Since the output voltage of converters is synchronized at 120□, so output voltage can be multiplied by three times.

According to phaser drawn the voltages

$$V_{a1\text{-}b1}\angle 0 = V_{b1\text{-}a2}\angle 0 = V_{a2\text{-}b2}\angle 0$$

Are all in phaseie phase difference is zero; thus, the output level is three times of the original.

We use similar converter and Hense control is very easy, this is the main advantage of cascaded n-multi-level converters are with x-mers which has standard supply 3-□ dual-level converter. But all the converters need SDCsource, and a x-mers is required to obtain the output voltages.

2. Diode-clamped multilevel inverter:
Several voltage-levels are achieved by using DCMI.Here we are going to determine the value of on-going NCP voltage differences. In case of even no. of voltage level, the neutral point is not accessible, and hence 'multiple point clamped' (MPC) is applied. In multi level system voltage balancing issue is faced so it is limited to three levels only.

In currently developing environment of industry, three level inverters are used for such purpose. Most of applications require medium voltage levels so we use 480V for application.

'Fig. 4.0indicate the topography of the 3-level diode-clamped inverter'.The three-level topology is more complicated than two level topology, but the operation is very easy and simple.

(a, b, or c) and

(d0, d1 ,d2)

"Are Phase -node connected to any node of the capacitor bank". Switching transistors Ta1 andTa2are are used to accomplisha phase connection by properly switching. The three states voltage levels are similar to the '2-level' inverter producing a LG (line to ground) voltage of zero or the dcvoltage.

For connection of junction d1 gate pulse are provided as

T_{a1}= off

T_{a2}=on.

The logical representation of off and onn means off=0 and onn=1. Both transistors switching sequences aresame so the table varies accordingly. Practically some dead time are provided between two consecutive applications, It means both transistors are switched of for a while. But theoretically this dead time are not calculated while calculation ie this dead time is ignored. According to the figure-2.5, it can be clearly observed, during switching , "the a-phase current ias will interin the nodefollowing diode as d.a1 whenit is -ve or comes out of the junction through diode Da2when the currents is are +tive". By observing such phenomenonTable 2.1 is drawn which is represented below.

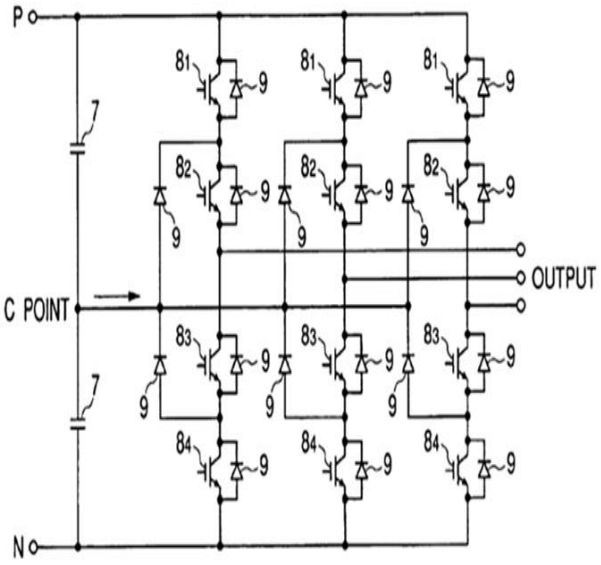


Fig 8. Diode Clamped Multilevel Inverter.

Table 1. Three level Inverter Relationships.

s_a	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}
0	0	0	0	0	0
1	0	1	v_{c1}	i_{as}	0
2	1	1	$v_{c1}+v_{c2}$	0	i_{as}

Table 2. Device Activation Stages.

Switching State	S_1	S_2	S_3	S_4	Inverter Terminal Voltage
P	On	On	Off	Off	E
0	Off	On	On	Off	0
N	Off	Off	On	On	-E

To calculate LG(line to ground) voltage capacitors are charged by 0.5 times of the DC voltage level. 'The dc currents iadc1 and iadc2 are the a-phase components to the junction currents in Figure 4 respectively'.

Switching level of each steps are provided by using n-level inverter which will be discussed in the next section. Transistor signals are provided by using gate signals to the transistors.

$$T_{ai} = \begin{cases} 1 & s_a \geq i \\ 0 & \text{elesewise} \end{cases} \quad \ldots\ldots\ldots\ldots 2.2$$

The inverse relation is shown by following equation

$$s_a = \sum_{i=1}^{n-1} T_{ai} \quad \ldots\ldots\ldots\ldots 2.3$$

To obtaina-phase vectors of the dc currents following expressions can be us

$$v_{ag} = \sum_{i=1}^{n-1} T_{ai}\, v_{ci} \quad \ldots\ldots\ldots 2.5$$

$$i_{adci} = \left[T_{a(i+1)} - T_{ai}\right] i_{as} \quad \text{for } i = 1, 2, \ldots (n-2)$$

$\ldots\ldots\ldots 2.6$

3. Flying capacitor structure:

Another fundamental multilevel topology is the flying capacitor. It usescascade-series-connection of capacit0r clamped switch-cells. This topology is lashed withmultiplenew and useful features in comparision to the diode-clamped inverter. Only one dc source is needed due to one of the inherited feature of flying capacitor inverteris redundancy within the phase auto balance the flying capacitors.

The operation of flying capacit0r benk is shown in fig.5.0.They are connected in such manner so that they

either add or subtract the voltage and for such purpose we add them in series connection. Table 2.2 represents the operationof the a-phase:

Table 3. Three level flying capacitors relationships.

s_a	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{adc}
0	0	0	0	0	0
1	0	1	v_{ac1}	$-i_{as}$	0
	1	0	$v_{dc} - v_{ac1}$	i_{as}	i_{as}
2	1	1	v_{dc}	0	i_{as}

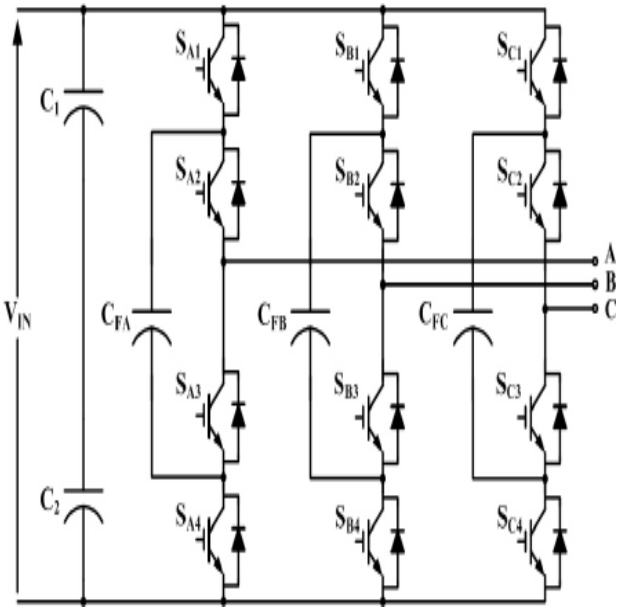


Fig 9. Three Level Flying capacitor Inverter.

Table 4. Switching Relationship of Three level flying capacitor.

T_1	T_2	T_1'	T_2'	V_{OUT}
1	1	0	0	E
1	0	0	1	E/2
0	1	1	0	E/2
0	0	1	1	0

One additional switching-level is obtained by using 3-level inverters. In addition, only2-transistor outputare used to make up the level sa. = 1 “letsassume the movement of the a-phase flycapacit0r current iac1to obtain the trivial state”, the charging or discharging state ofthe capacitor can be considered and Hens the capacitor-voltage can be regulated-to it’srequired quantity by switching among the phases. “In Table 2.2, the current iadc is the a-phase component of the dc current”. The net dc-current may be obtained by adding the components of all the three phases.

The charge of the capacitor is un-affected by the different states of the flying capacitor inverter. 2 different inter-mediate voltage levels may be obtainedby examining enough deadzone that all capacitors can be changed to their ideal voltages.

n-level equation for flying capacitor inverter are given below

$$v_{Tai} = (1-T_{ai})\left[v_{aci} - v_{ac(i-1)} - I_a v_{sw} + (1-I_a)v_d\right] + T_{ai}\left[I_a v_{sw} - (1-I_a)v_d\right]$$

……2.6

IV. MODULATION CONTROL SCHEMES

The prime motive of the project is to collect the required and useful info on n-level inverter topologies and its modulation technique. From the literature evaluation three non-identicaln-level inverter topography proposed and one of the topography are selected as the motive of the project for analysis in terms of methods and char.

MATLAB/Simulink blocks are used to construct this MLI(multi-level-inverters) topography and the modulation technique. Simulation of both MLI (multi-level-inverters)ensureproduction of the related output voltages wave-forms which are useful to determine the common data for more analysis purpose.

1. Control Strategy (Modulation Methods):

Each operations of inverter’s to reproduce an acvoltagesobtained by dc sources, the semi-conductor switcheshould be alternatedin-between the 2 state low or high in well-organized and the time-sequence manner for generation ofac-supply which represents+ve and -vepartof a dc source only 1 portion .This is obtained by using different control technique and modulation modules that will be used to manipulate and trigger the inverter switch at unlike time sequence.

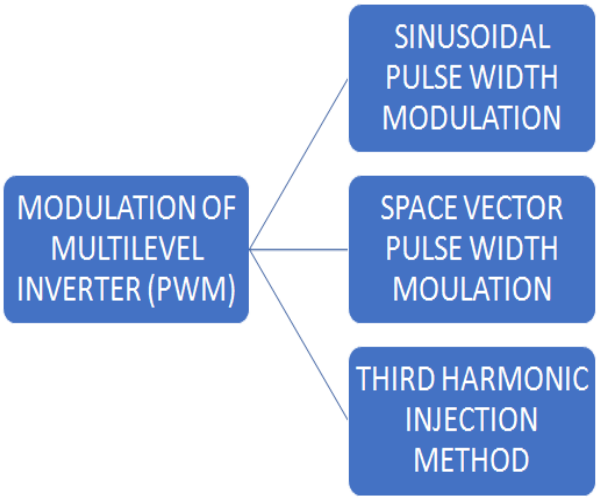


Fig 10.**Types of modulation techniques.**

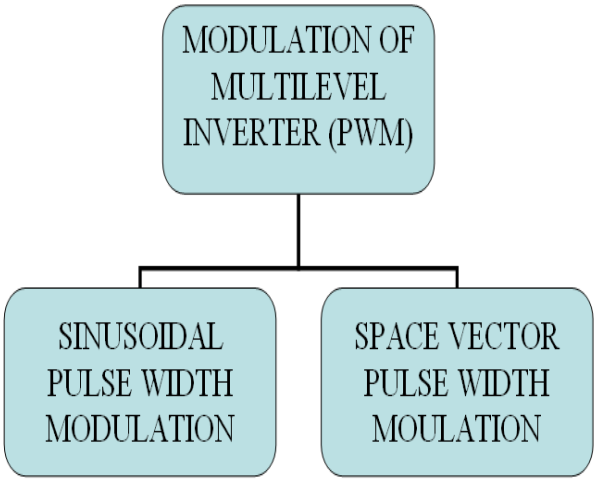


Fig 11. Types of modulation.

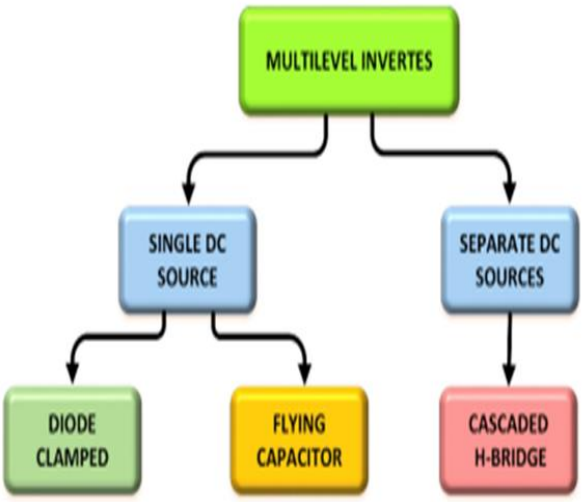


Fig 12.**Multilevel inverters Classification.**

2. Space vector pulse width Modulation method (SVPWM):

In the previous chapter 2.3 it has been discussed that an ac voltage wave form can be produced with the help DCMLI. This inverter consists of clamping diode with a capacitor. There are several methods of control strategy and device commutation techniques are present for multilevel NPC. The capacitor cascaded split the inverter input voltage including a floating neutral point.

The working status of the semiconductor switches are in the NPC is under stable bytwo cases

- Case 1 Where switching indicates P:
- Case 2 Where switching indicates O:
- Meansthe output voltage iszero.

[P], [O], and [N] are the tree operation status shown by each inverter leg with this three possible switching condition a total of 27 possible mixtures can be made and described in Table 4.1, the switching state may be described as below (by the help of alphabets A B C).

To derive the relation between switches Space Voltage Vectro is classified into four groups.

- **Zero Vector (V0),** is expressed by the three switching states [PPP], [OOO], and[NNN]. The magnitude of V0= 0.
- **Small vectors (V1 to V6),** All gain a magnitude of Vd / 3 (QWhereVd is the DC voltage).
- **Medium vector (V7 to V12),** Havingmagnitude of √3Vd/3.
- **Large vector (V13 to V18),** All containing a magnitude of 2Vd/3.

Table 5. Voltage vector and switching states.

Space vector		Switching State		Vector classification	Vector magnitude
		P - type	N -type		
V_0		[PPP][OOO][NNN]		Zero vector	0
V_1	V_{1P}	[POO]		Small vector	$1/3V_d$
	V_{1N}		[ONN]		
V_2	V_{2P}	[PPO]			
	V_{2N}		[OON]		
V_3	V_{3P}	[OPO]			
	V_{3N}		[NON]		
V_4	V_{4P}	[OPP]			
	V_{4N}		[NOO]		
V_5	V_{5P}	[OOP]			
	V_{5N}		[NNO]		
V_6	V_{6P}	[POP]			
	V_{6N}		[ONO]		
V_7		[PON]		Medium vector	$\sqrt{3}/3V_d$
V_8		[OPN]			
V_9		[NPO]			
V_{10}		[NOP]			
V_{11}		[ONP]			
V_{12}		[PNO]			
V_{13}		[PNN]		Large vector	$2/3V_d$
V_{14}		[PPN]			
V_{15}		[NPN]			
V_{16}		[NPP]			
V_{17}		[NNP]			
V_{18}		[PNP]			

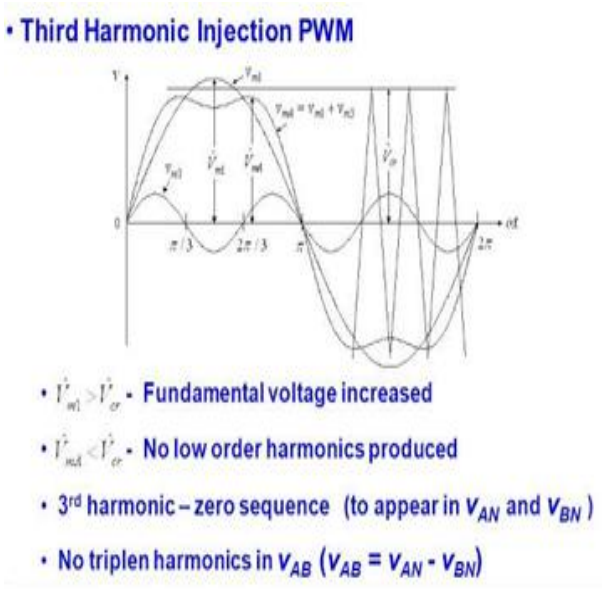
3. Third harmonic Injection method:

SPWM methods are used for injection of the voltage so that we can eliminate the third harmonic content. The fundamental voltage is magnified by use of 3rd Harmonics to the 3-phase sinusoidal modulating signal without over modulating the wave signa.

Fig describes the working of this Pulse width modulation scheme, here the modulating signal isv.mA is the

fundamental wavevm1 and a 3rd harmonic component vm3, and the resulting in flatted top signal. This causes fundamental signal "Vm1 greater than the tri-angular carrier wave Vcr,"which boosts the fundamental signal. To avoid over modulation the carrier signal should kept low.

In the upcoming chapter the detail analysis of third harmonic injection to the diode clamped inverter will be discussed. The analysis has been done by MATLAB simulation and their corresponding results are given in the upcoming chapters.



4. SPWM-Methods:

The modulating signal has a sine wave of frequency f.m and amp A.m.where reference sine wave signal compared with square wave carrier signal to produce gate signal that can be applied to the invert gates.

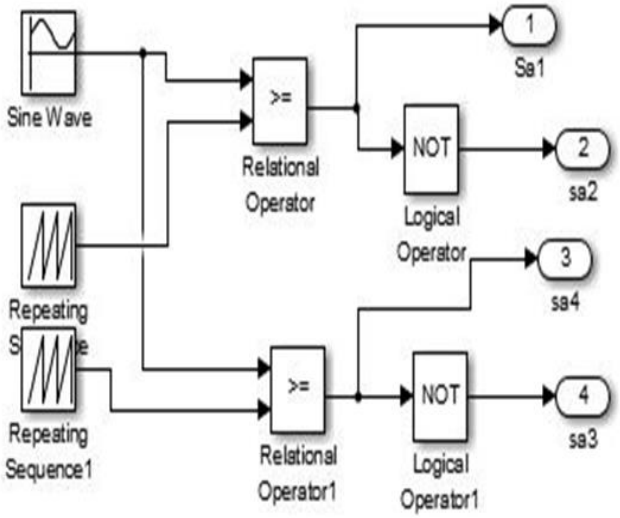


Fig 13. The PWM circuit of one bridge inverter.

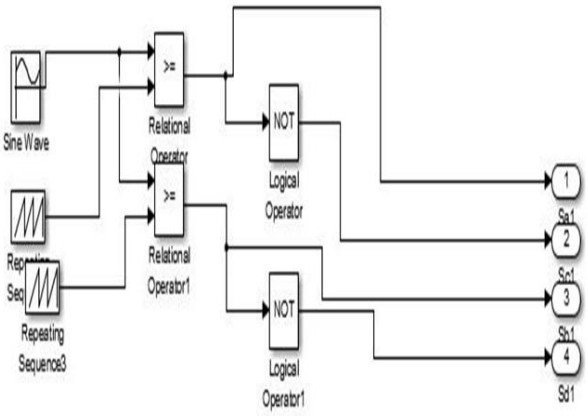


Fig 14. SPWM for one leg 3-level diode clamped inverter.

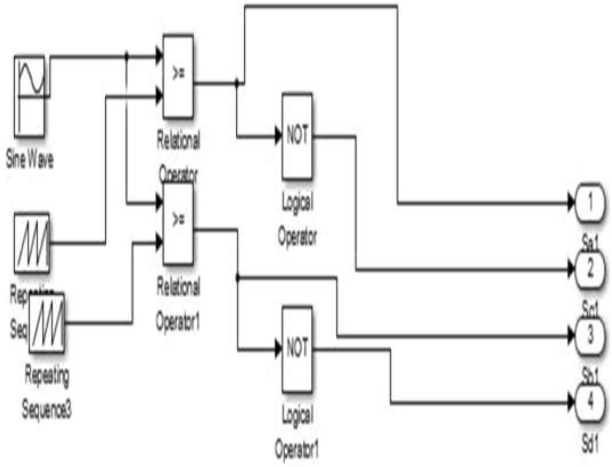


Fig 15. The gate signal for one leg 3-level flying capacitor inverter.

The SPWM concept is to compare the reference sine wave with set of carrier wave and by using additional logic gates the desired switching sequence can be achieved The concept behind the SPWM is that sine wave is compared with square wave signal to produce the gate signals that control the inverter as shown in figure

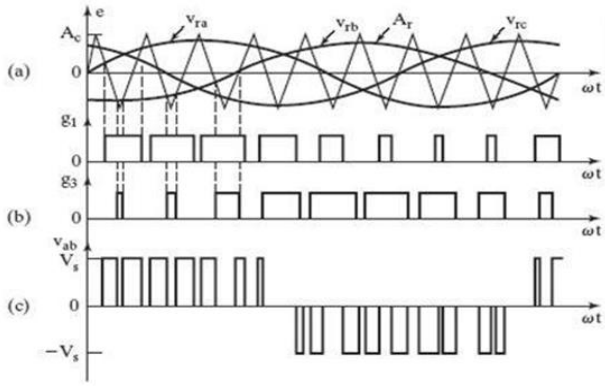


Fig 16. The SPWM modulation techniques for three phase inverter.

5. Implementation using MATLAB/Simulink:
Diode clamped multilevel inverter: The three level diode clamped multilevel inverter circuit is shown in figure 9 which has been built using Matlab /Simulink

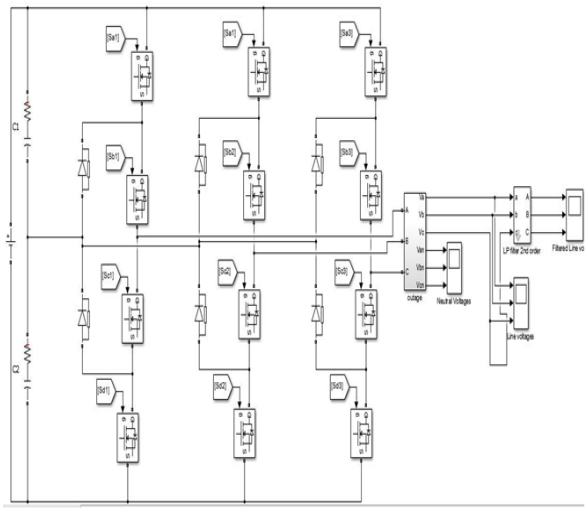


Fig 17. 3-level diode clamped multilevel inverter circuit design.

V. PV ARRAY AS DC INPUT IN MULTILEVEL INVERTER

1. Introduction of PV array:
A PV array is a smart combination of solar cells, which is connected either in series or parallel configuration to extract solar energy into usable electric power. The quantity of power can be boosted by adding the number of solar cells. The maxmpower can be tracked by using various MPPT tracking algorithms. In the fig no.14 we can the PV cells, modules, panels and arrays.

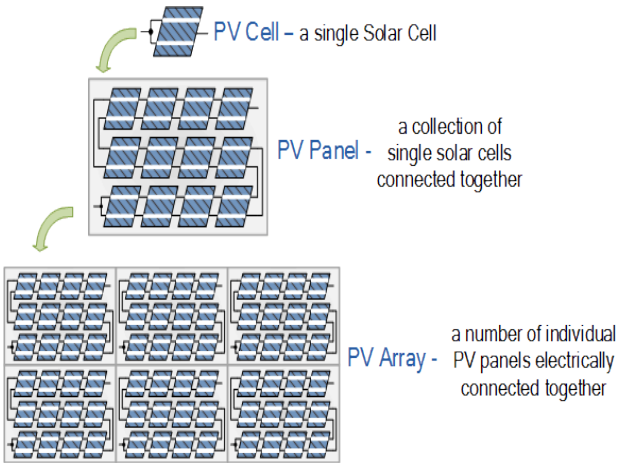


Fig 18.**PV Array.**

The PV- panels are constructed of individual cells arranged together, then the Solar PV-Array. The array is also made by arranging solar panels as shown in the above figure. The arrays are constructed to increase the power generation capability if we increase the area of the array the generating capacity also increase.

Now days the main renewable source is solar and a complete PV-array is the main source to generate solar energy. Most manufacturing companies procure standard PV panels of the voltage rating of 12V to 24V.Now if we want to increase the output voltage the panels must be connected in series or parallel arrangements.

2. Benefits of using PV array as input of MLI:
Since during the last decade the PV system has become one of the most favored renewable and sustainable energy sources, it is most environment friendly and sustainable energy source.The insolation energy from the sunlight is used as energy source for the PV array. The output of the PV array is a DC signal and this signal is utilized as a input source for the MLI (Multi level Inverter).

Solar array can convert solar radiation into electrical energy to provide the required energy for input to the NPC which has been considered here.solar energy is one of the most popular and research area for few decades for both gird-connected and standalone applications.

In most of the PV-fed inverter the dc input is given from dc supply. A solar PV panel is constructed by connecting solar cells in series and parallel to achieve required voltage and current. In my simulation model 40 parallel and 12 series modules are connected. Each solar cell has a rating of .5 volt and 8 amp. In standard test conditions of 1000W/mm2 and 250C.In this paper DCMLI topologies are reviewed because of their lucidity.

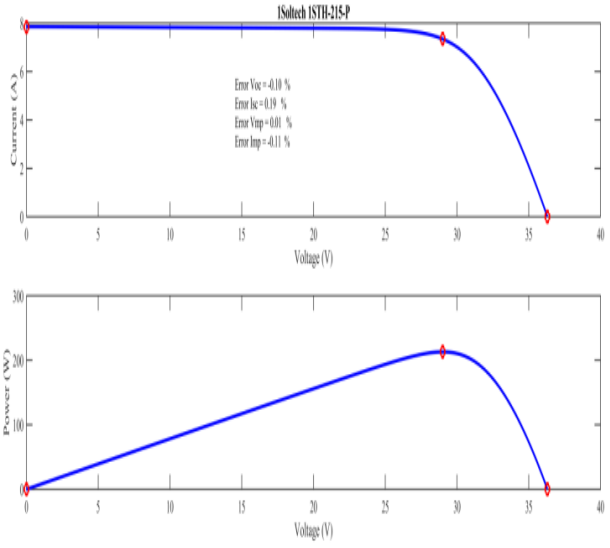


Fig 19.Output waveform of PV Module.

In the above fig. V-I & P-V char. of the PV module designed on the MATLAB.

International Journal of Scientific Research & Engineering Trends
Volume 8, Issue 1, Jan-Feb-2022, ISSN (Online): 2395-566X

VI. PRELIMINARY SIMULATION RESULTS

Figure 10 and figure 11 show the output line and phase voltages for three level diode clamped multilevel inverter (DCMI) by using SPWM modulation technique and figure 12 shows the harmonics content and THD %

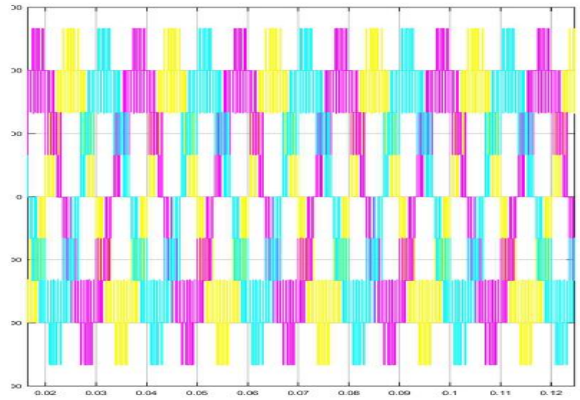


Fig 20. Output phase voltage.

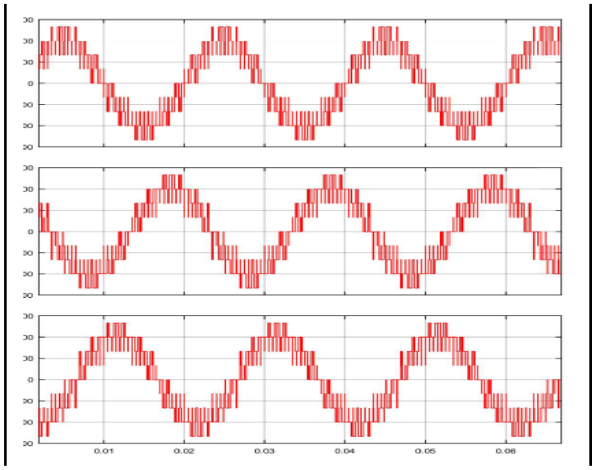


Fig 21. Output Phase voltage.

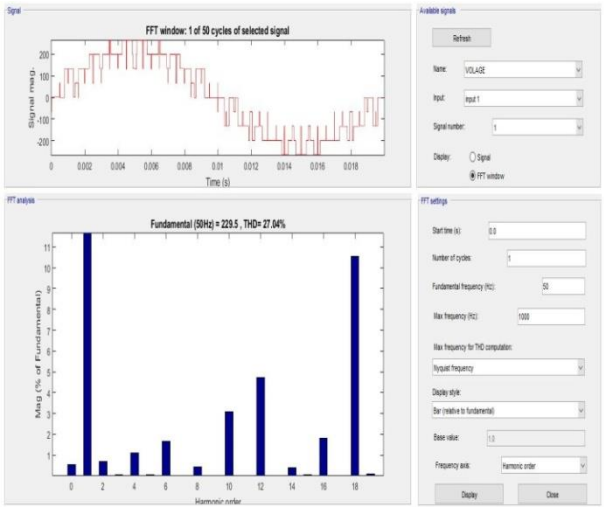


Fig 22. Output %THD in voltage signal.

Table 6.Inverter description table.

Type of Inverter	No of Level	Carrier Freqency	Thd%	Technique
Dcmli	3	1000	27.04	Pwm
Inverter Type	No of Switches	No of Cpacitors	No of Diodes	Total Components
Dcmli	3	2	6	20

VII. SUMMARY

We have successfully discussed the study conducted on three-levelsinvetor topologies CHMLI, DCMLI and FCMLI and using MATLAB/Simulink on DCMLI. The date obtained from the simulation results was tabled and compared in terms of different aspects. Now to reduce the losses, harmonic content we have to increase the level and decrease the used component.

REFERENCES

1. Bin-wu in his book “High Power Converters and Ac Drives”
2. Nabae, I Takahashi and Akai in their paper “A New Neutral Point Clamped PWM Inverter”.
3. Cheng-Han and Tsorng in their experimental paper “Design and Implementation of a Novel multilevel DC-AC inerter”.
4. R. A Ahamed, S. Mekhilef and W. P. Hew , “New Multilevel inverter topology with minimum no. of switches”
5. Ahmet M Hava has discussed different carrier based PWM techniques
6. De Soto, W., Klein, S.A., Beckman,W.A., Improvement and validation of a model for photovoltaic array
7. An Altered PWM Strategy for Over modulation Operation of Three-Level NPC Inverter with Capacitor Voltage Balancing Santu Kr. Giri* , Student Member, IEEE, Sarbani Mukherjee* , Student Member, IEEE, Sourabh Kundu† , Student Member, IEEE, Subrata Banerjee† , Senior Member, IEEE
8. Comparative Analysis of Close Loop Three Level Voltage Source Inverter Using Sinusoidal Pulse Width Modulation And Third Harmonic Sandeep Ojha, Chanchal Sharma, Ashok Kumar Pandey
9. De Soto, W., Klein, S.A., Beckman,W.A., Improvement and validation of a model for photovoltaic array performance. Sol. Energy 80(1), pp.78-88, 2006.
10. R.KameswraRao,P. Srinivas,M.V.Suresh Kumar “ Design and analysis of variousInverters using different PWM Techniue”
11. N. Mohan, T.M Undelandetal. “Power Converters, Applications and Design” 3rd Edition, Johan Wiley and Sons, NewYork,2003.

12. Raja Ram Kumar, Sunil Kumar, Alok Yadav, "Comparion of PWM Techniques and Inverter Performance" ISOR Journal of Electrical and Electronics Engineering(IOSR-JEEE), ISSN:227-1676 Vol 4,Issue 1(Jan-Feb 2013),PP 18-22
13. J. Holtz, "Pulse width modulation for electronic power conversion," Proc. IEEE, pp. 1194–1214, Aug. 1994.
14. H. W. Van Der Broeck, "Analysis of the harmonics in voltage fed inverter drives caused by PWM schemes with discontinuous switching operation," in European Power Electronics Conf. Rec., 1991, pp. 261–266.
15. G. Buja and G. Indri, "Improvement of pulse width modulation techniques," Archivf˙urElektrotechnik, 57, pp. 281–289, 197516. S. Jul-Ki and S. Sul, "A new over-modulation strategy for induction motor drive using pace vector PWM," in Applied Power Elect. Conf.,Dallas, TX, Mar. 1995, pp. 211–216.
16. DATTA, S.M."Power Electronics & Control". Reston, VA: Reston Publishing Co., Inc., 1985
17. Zheng, H., Li, S., Bao, K., et al.: 'Comparative study of maximum power point tracking control strategies for solar PV systems'. IEEE Conf. on Transmission, Distribution and Exposition, May 2012, pp. 1–8
18. Leon M. Tolbert, John Chiasson, Keith McKenzie, Zhong Du, Elimination of harmonics in a multilevel converter with non-equal DC sources, IEEE transaction on Industry applications, Vol.41, 2005
19. José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng, Multilevel Inverters: A Survey of Topologies, Controls and Applications, IEEE transaction on Industry Electronics, Vol.49, 200221.
20. Leon M. Tolbert, Fang Z. Peng, Multilevel Converters as a Utility Interface for Renewable Energy Systems, Power engineering society summer meeting, 2000, IEEE
21. D. Grahame Holmes, Thomas A.Lipo, Pulse width modulation for power converters, 2003 by Wiley interscience Inc.
22. Muhammad H. Rashid, Power Electronics circuits, devices, and applications. 2004 by Pearson education Inc.
23. M.Nivachini, C.Vidhya, S.Suresh, Implementation of New Single PhaseMultilevelInverter for Grid Connected PV Power System, International Conference on Emerging trends in Computer and Communication Technologies EMICS'12 on 16-17 Feb. 2012, Maria College of Engineering and Technology, Kanyakumari, (2012).