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Review of Design multiplexer using QCA

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Abstract: -A novel design of a quantum-dot cellular automata (QCA) 2 to 1 multiplexer is presented. The objective is the development of a modular design methodology which can be used to design 2n to 1 multiplexers using building blocks. For the QCA implementation a careful consideration is taken into account concerning the design in order to increase the device stability. The proposed multiplexer is designed and simulated using the QCADesigner tool.

Keywords - quantum-dot cellular automata, circuit design, circuit simulation, multiplexers, nanoelectronics

I. INTRODUCTION

Microelectronics industry for more than 40 years has benefited from great improvements in terms of speed and size of electronic devices. One nanostructure paradigm, originally proposed by Lent et al. [1], [2], is Quantum-dot Cellular Automata (QCA), which make use of arrays of coupled quantum dots [15] to put in operation Boolean logic functions. Conventional digital technologies use ranges of voltage or current to represent binary values. In contrast, QCA uses the position of electrons in quantum dots to represent binary values '0' and '1'. The primary advantage of QCA is the exceptionally high packing derived from the small size of dots along with the interconnection simplicity and the notably low power-delay product [5].

The basic building block of QCA devices is the QCA cell shown in Figure 1(a). A QCA cell consists of several quantum dots with two mobile electrons. A quantum dot is a region in the cell structure where charge can localize. Coulomb repulsion between the electrons will force them to occupy antipodal sites in the square. For an isolated cell, there are two energetically equivalent arrangements of the extra electrons that are denoted as state polarization P. The cell polarization is used to encode binary information. A polarization of P=+1 (Binary 0) results if cells 1 and 3 occupied, while electrons on sites 2 and 4 result in P=-1 (Binary 1) as shown in Figure 1(b).

The polarization of non-isolated cell is determined based on interaction with neighboring cells [4], [6]. It is possible to implement all combinational logic functions by properly arranging cells so that the polarization of one cell sets the polarization of a nearby cell [14]. According to previous studies several logic gates and computing devices [10] are implemented with QCAs. Basic implementations have been proposed are: the binary wire [2], the majority gate, AND gate [3], OR gate [3], NOT gate [3], XOR gate [3], full adder [3], [7], multiplexer [7], [8], Arithmetic Logic Unit (ALU) [7], Serial memory [13] etc.

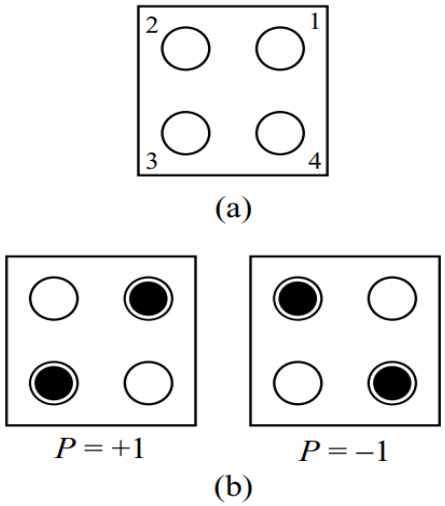

Fig.1: The basic four dot QCA cell.

In this paper the design and simulation of a QCA 2 to 1 multiplexer is presented. The proposed QCA multiplexer designed and simulated by using the QCADesigner tool. QCADesigner is a QCA layout and simulation tool developed at the University of Calgary [16].

II. MULTIPLEXER DESIGN

In general, an electronic multiplexer makes it possible for several signals to share one expensive device or other resource, for example one A/D converter or one communication line, instead of having one device per input signal. As a result, the multiplexer is an extremely important part of signal control systems, because it allows the system to choose one of several inputs to be forwarded to one output [17]. The selection bus determines which input signal is allowed to pass through to the output unchanged. In this paper we present the design and simulation of QCA 2 to 1 multiplexer in order to explore design methods for designing 2n to 1 multiplexers.

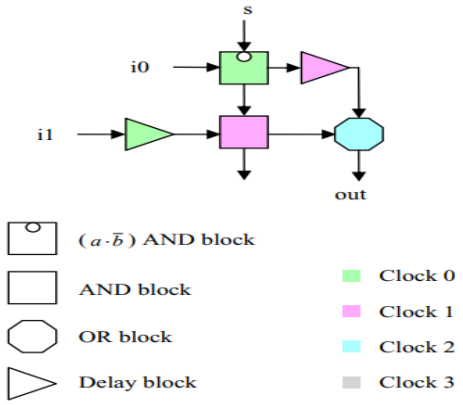

Fig.2: High-level block diagram of 2 to 1 multiplexer.

The main objective is to develop a modular design methodology which can be used to design 2n to 1 multiplexers using building blocks. To meet this specification the design must consist of elementary blocks properly selected so that can be used to build larger 2n to 1 multiplexers. A high-level block diagram of the 2 to 1 multiplexer design is shown in Figure 2, where i_0 and i_1 are the multiplexer signal inputs, s corresponds to the selector input and out is the multiplexer output signal.

The design includes an AND block, an (·ba) AND block and an OR block. It also includes one signal delay block at the i1 input of the circuit. All blocks are coloured according to the clock they use. It can easily be seen that the clocking phases are traversed in the proper order (0, 1, 2, 3, 0, 1, …) so that the required clock phases are always adjacent to one another to allow for correct signal propagation. The signal propagates diagonally with a line profile from the top left block to the bottom right block which is the output block. Please, leave two blank lines between successive sections as here. Using this pipelining structure the proper signals arrive simultaneously at the inputs of the AND and OR blocks. The signal delay block must exist at the i1 input in order to synchronise the first column AND block west input signal, with the s signal coming from the north input which already has been delayed from the previous level AND block.

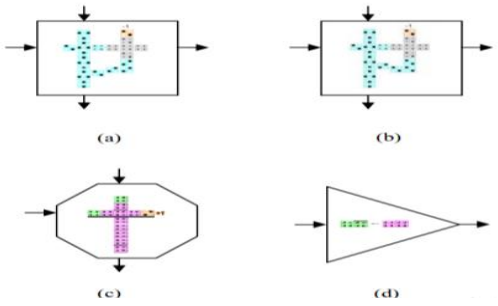

Fig.3: Elementary blocks layout implementation of the 2 to 1 multiplexer design, (a) AND block, (b) (·ba) AND block, (c) OR block, and (d) Delay block

Figure 3 shows the implementation of the AND, (·ba) AND, OR and signal delay blocks. Both AND and (·ba) AND blocks consist of one majority gate with the first input fixed to logic 0 implementing an AND gate for the other two inputs.

The second input of majority gate is evaluated from the west input and the third input of majority gate is evaluated from the north input of the block. The north input of the block walks vertically the block crosses the horizontal line comes from the west input and fans out to the south output of the block and to the third input of majority gate. The output of the majority gate arrives at the east output of the block. AND and (·ba) AND blocks layout presenting in Figure 3(a) and 3(b) illustrate a useful feature of QCA design, namely the ability to cross wires in a two dimension design. In conventional technology, information is coded in voltages or currents in conductors and wire crossings require the presence of a bridge to avoid electrical contact. Using QCA wires, signals can be crossed in the same layer by employing 45o rotated QCA cells. The vertical line in the block from north input to the south output is a wire of such rotated cells. Because of their diagonal orientation, their polarizations alternate down the line (an inverter chain).

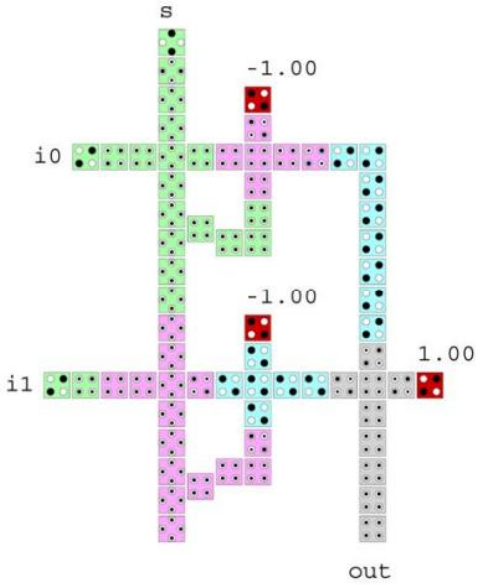

Fig.4: Final QCA implementation of the 2 to 1 multiplexer.

The main advantage in using such lines for signal propagation is that the normal wires can be crossed without interference or crosstalk. Furthermore, because of the alternating polarization, both the signal and its complement are easily extracted. In the presented design the evaluation of the third input of the majority gate is succeeded by the the extraction of the same polarity of the north input signal from the inverter chain for the AND

block, and the complement of the north input signal for the (·ba) AND block, respectively.

The OR block layout implementation is presented in Figure 3(c). It consists of one majority gate with the first input stetted statically to logic 1 and implements an OR gate for the other two inputs corresponding to the north and west input of the block. Finally, the Delay block layout implementation is presenting in Figure 3(d). In a Delay block the input signal is delayed by one quarter clock period. In the proposed implementation the aforementioned block consists of two pairs of cells connected serially resulting in a line. Clocking phases of the pairs are traversed in the proper order (0, 1, 2, 3, 0, 1, …) so that the required clock phases are always presented at the proper sequence in order propagate the signals correctly and produce signal delay equal to the number of the included cell pairs. The reason for using two cells clocked to the same phase for every quarter of clock delay, is to isolate the state of every pair from the state of the cell located next to the output of the delay block.

The final QCA implementation layout of the proposed 2 to 1 multiplexer is presented in Figure 4. The design consists of 67 cells covering an area of 0.14 um2 . The simulation results of the design are presented in Figure 5. The multiplexer's simulation was performed with the help of the QCADesigner tool [16]. In QCA implementations it is very important to produce a design which is operationally stable. There are some design concerns kept into account to increase the design stability [9]. When generating designs in QCA, a significant effort should be made to keep the length of a wire within a given clocking zone to a minimum. The reasons to do this is that as wire length grows, the probability that a QCA cell will switch successfully decreases in proportion to the distance a particular cell is from a frozen input at the beginning of the wire. Consequently, for shorter wires, it is most likely that all cells making up the wire will switch successfully. Additionally, taking into account short wire lengths, the presented design can operate in higher clock rates.

This is because, before a given zone can change phase, every cell within the zone must make appropriate polarization changes, so the longer the wire, the longer the time for a signal to propagate down the length of it. The maximum wire length in the proposed design equals to 10 cells. Furthermore, it is well known that the design robustness depends on the non uniformity of cell distribution in clocking zones. For example, if the clocking zones consist of a great number of cells the corresponding design can only operate in very low temperatures because of thermodynamic effects. In the presented design the use of clocking zones with many cells is avoided and consequently the QCA cells are uniformly distributed into the clocking zones.

Another problem arising with complex QCA designs is that usually the designs are not distributed uniformly in the area and a large amount of white space-wasted area is wasted between cells [11]. To confront with this problem, the total area covered by QCA cells was minimized by keeping the distance between binary wires as close as possible according to QCA design rules proposed by Kyosun Kim et.al. [9], [12] As a result, the proposed architecture does not leave large amount of area unused.

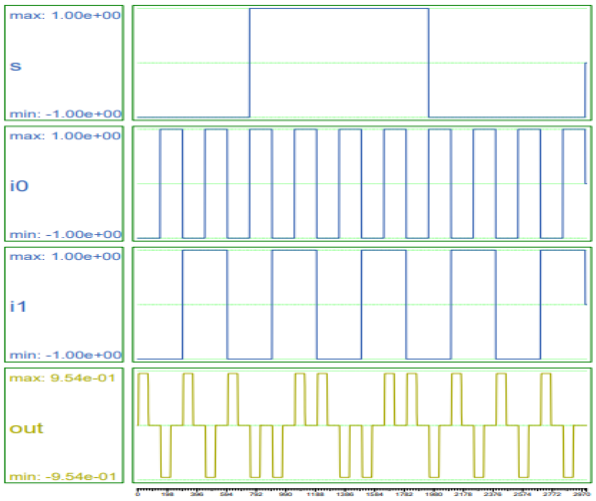

Fig.5: Simulation results of the 2 to 1 multiplexer design.

III. CONCLUSION

The multiplexer is an extremely important part of signal control systems, as well as in nanoelectronic circuits, because it allows the system to choose one of several inputs to be forwarded to one output. In this paper the design and simulation of 2 to 1 QCA multiplexer was presented in order to explore design methods for designing 2n to 1 multiplexers. A modular design which can be used to extend 2 to 1 multiplexer QCA layout to larger 2n multiplexers layouts, using the elementary building blocks has been proposed. The resulting design consists of 67 cells covering an area of 0.14 um2 . The simulation in this work has been carried out using the simulator included in the QCADesigner tool, at zero temperature.

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