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Designing Of Power and Delay Efficient 10T and 14T SRAM Cell

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***Abstract*- This work presents an analysis of popular 1-bit full adder circuits. The analysis metrics comprised of power, delay, power-delay-product, area, and threshold loss. As an important unit of various hardware computational blocks, the transistor level design of the full adder circuit has been evolving for decades. In this comparative study, we focus on the highly cited designs of last two decades. This paper presents design of a new stable and 14T full power efficient adder circuit. The proposed circuit is designed based on Pass Transistor Logic (PTL) network using NMOS transistor only. The proposed circuit is simulated at layout level using LTSpice tools technology in terms of power and voltage level at the sum and carries nodes. The proposed circuit performance is compared with a similar 14T adder circuits and found the proposed adder circuit consumes lower power due to smaller load capacitance and parasitic resistance. The logic level at the sum and carry nodes maintains at strong 1 or strong 0 due to proposed circuit's design architecture.This paper we introduced 10T one-bit full adders, and 14T including the most motivating of those are analyzed and compared for speed, leakage power, and leakage current. The analysis has been performed on various process and circuits techniques, the analysis with minimum transistor size to minimize leakage power, the latter with simulate transistor dimension to minimize leakage current. The simulation has been carried out on a LTSPICE tool using a .065nm technology. 10T adder and 14T adder.**

***Keywords* -Pass Transistor Logic (PTL),LTSpice tools,10T and 14T SRAM**

I. INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU. They are also used in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators and similar operations. Although adders can be constructed for many number representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require more logic around the basic adder. The half adder adds two single binary digits A and B. It has two outputs, sum (S) and carry (C).

The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2C + S. The simplest half-adder design, pictured on the right, incorporates an XOR gate for S and an AND gate for C. The Boolean logic for the sum (in this case S) will be A′B + AB′ whereas for the carry (C) will be AB. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.[1] The half adder adds two input bits and generates a carry and sum, which are the two outputs of a half adder. The input variables of a half adder are called the augend and addend bits. The output variables are the sum and carry.

Necessity of Low Power Arithmetic Circuits - Arithmetic circuits find numerous applications in architectures proposed for signal and image processing. As the complexity of Digital Signal Processing (DSP) architectures is relatively higher, low power design techniques are now emerging. The data published in 1997 edition of National technology roadmap for Semiconductor Industries Association (SIA) predicted that the complexity of microprocessors would be doubled for every twelve months as stated by Gorden Moore in 1965.

Although this time line varies upto 24 months, regardless of the exact numbers, it is agreed that the growth rate is rapid. New processing technologies are being developed, while the present generation devices are at a very safe distance from the fundamental physical limits. A need for low power Very Large Scale Integration (VLSI) chips arise from such an evolution. For example, the Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then came Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2.40 GHz (Sharma 2012). While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size

of the integrated circuits. If this exponential rise in the power density increases continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor(Sharma 2012). Such high power density introduces reliability concerns such as, electro-migration, thermal stresses and hot carrier which induce device degradation, resulting in the loss of performance.

Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly increases the low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. Digital systems such as note book computers, cellular phones and personal digital assistants are running on batteries. For these systems, low power consumption is a prime concern, because it directly affects the performance of the battery longevity.

II. RELATED WORK

In addition, the smaller size transistors (technology scaling) not only allow integration of large number of components on a chip, but also reduce the signal propagation delay which in turn permit higher clock frequencies at the expense of leakage power dissipation. However larger number of devices on a die, results in an overall increase in power dissipation posing special challenges on heat dissipation, i.e. cooling and packaging technology. This necessitates the need to orient the research towards reducing area and power dissipation in VLSI circuits used in ALUs and MAC units of processing architectures.

SomashekharMalipatil et.al (2020) GDI (Gate Diffusion Input) is a new technique of low power digital circuit design is proposed. This technique allows minimization of area and power consumption of digital circuits. In this design XOR gate is designed using 3 transistors and CMOS full adder is designed based on two 3T XOR and one 2T Mux. Using 8 transistors the full adder is designed in this paper and voltage scaling also done by reducing supply voltage. In this proposed full adder, the power consumption 4.604μW is achieved and the total area is 144μm 2 .

M. Keerthana et.al (2020) Adders are plays a vital role in digital and vlsi systems. Arithmetic operations are an essential part of digital systems. During VLSI systems, the entire research is on lowering the scale of transistors for enforcing any other digital system. This proposed architecture implemented by different types of logic systems; each logic performs the different role in the hybrid system. The hybrid Full Adder cell with one bit is implemented in this structure. The proposed method is investigated using 22-nm CMOS hybrid full adder. The proposed architecture demonstrates substantial efficiency in power consumption and delay, based on simulation results. The simulation result expressed that the full adder circuit is used to modern high speed central processing unit in the data path architecture. This form of hybrid Full Adder, reduces the delay and increasing efficiency and mainly used in nano technology applications. The average power consumption of 1.1055 μW with moderately low delay of 7.0415ps was found to be extremely low for 0.8-V supply at 22-nm technology. These kind of adder allocates significant improvements in power, high speed and area compared with previous full adder designs.

Boopathy. E Veera et.al (2018) Using multioutput domino CMOS logic, a cost effective implementation of Manchester carry chain (MCC) adder for 8-bit is designed in this paper. From this adder carries are generated parallelly employing two main carry chains of 4-bit. The suggested 8-bit adder module comprise confined length of carry chain. As a result of this ability, it is applied to realize broader adders and as well it guides to betterments in functioning rate equated to the related adders established upon the classical 4-bit MCC adder module.

Problem formulation

This process a novel scheme for 8T SRAM memory location write and read operation process using CMOS technology.

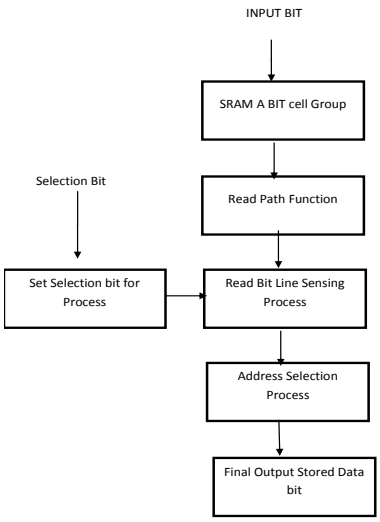
- It is necessary to ensure any leakages which cause the read sensing failure and degraded cell stability due to the half-select write.
- For avoid this situation proposes an equalized bit line scheme to eliminate the leakage dependence on data pattern and thus improves RBL sensing.

Also this process a fast local write-back (WB) technique to implement a half-select-free write operation. With hierarchical bit line architecture, it facilitates a local read and a subsequent fast WB action to secure the original data without performance degradation

III. PROPOSED APPROACH

A propose an 10T and 14T SRAM cell implementation, previously used for improved read speed.Isolating the read path from internal storage nodes. The inverter (M6 and M7) is driven by node QB and drives the read bit line (RBL) through TG (M8 and M9) which is controlled by two complementary read word lines (WLs). This 10T and 14T cell can fully charge or discharge RBL by itself during a read operation. Thus, it is totally unnecessary to prepare a pre-charge circuit for RBL. The dynamic power is consumed on RBL just when the read datum is changed. That is to say, the dynamic power dissipation on RBL is zero if consecutive “0”s or consecutive “1”s are read out. Non-destructive column-selection-enabled 10T SRAM for aggressive power reduction is presented in this brief. It

frees a half-selected behaviour by exploiting the bit line-shared data-aware write scheme. The differential-VDD (Diff-VDD) technique is adopted to improve the write ability of the design. In addition, its decoupled read bit lines are given permission to be charged and discharged depending on the stored data bits.



Full adder- A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full-adder adds three one-bit numbers, often written as A, B, and Cin; A and B are the operands, and Cin is a bit carried in from the previous less-significant stage.[2] The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. The circuit produces a two-bit output. Output carry and sum typically represented by the signals Cout and S, where the sum equals 2Cout + S. A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates. One example implementation is with S = A ⊕ B ⊕Cin and Cout = (A · B) + (Cin· (A ⊕ B)). In this implementation, the final OR gate before the carry-out output may be replaced by an XOR gate without altering the resulting logic.

Using only two types of gates is convenient if the circuit is being implemented using simple integrated circuit chips which contain only one gate type per chip. NOR Full adder A full adder can also be constructed from two half adders by connecting A and B to the input of one half adder, then taking its sum-output S as one of the inputs to the second half adder and Cin as its other input, and finally the carry outputs from the two half-adders are connected to an OR gate. The sum-output from the second half adder is the final sum output (S) of the full adder and the output from the OR gate is the final carry output (Cout).

The critical path of a full adder runs through both XOR gates and ends at the sum bit s. Assumed that an XOR gate takes 1 delays to complete, the delay imposed by the critical path of a full adder is equal to T_FA=2 . T_XOR=2D The critical path of a carry runs through one XOR gate in adder and through 2 gates (AND and OR) in carry-block and therefore, if AND or OR gates take 1 delay to complete, has a delay of T_c=T_XOR+T_AND+T_OR=D+D+D=3D.

Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

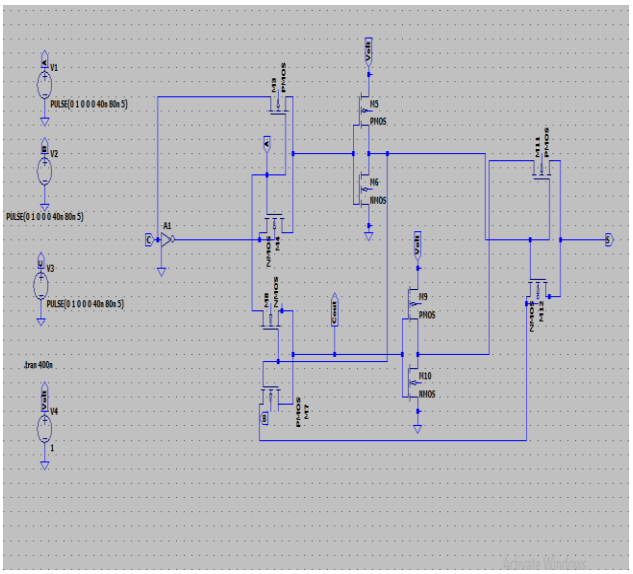


Fig 1 Simulation Circuit PTL based 10T full adder

The full adder is a part of the critical path that determines the overall performance of a system. So the overall performance is dependent on adder performance. I-bit full adder is one of the most critical components of a processor that determines its throughput. In this work we have designed a new I-bit 10- transistor full adder which consumes less power than the standard implementations of full adder cell. The proposed adder cell is simulated and compared with the other 10- transistor adder cell and other transistor cell under the same conditions. The addition of 2 bits A and B with Cin yields a SUM and a CARRY bit.

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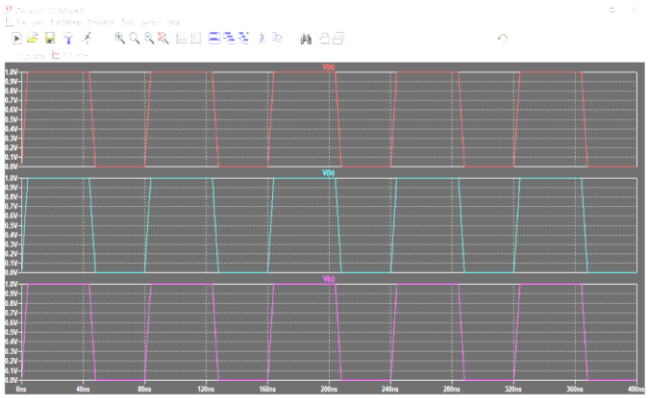

Fig.2 Input Waveform Of PTL based 10T full adder

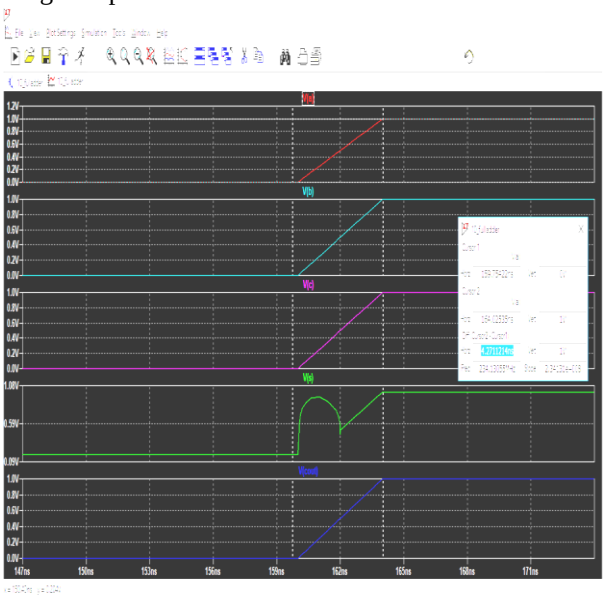

Fig 3 Delay of the PTL based 10T full adder.

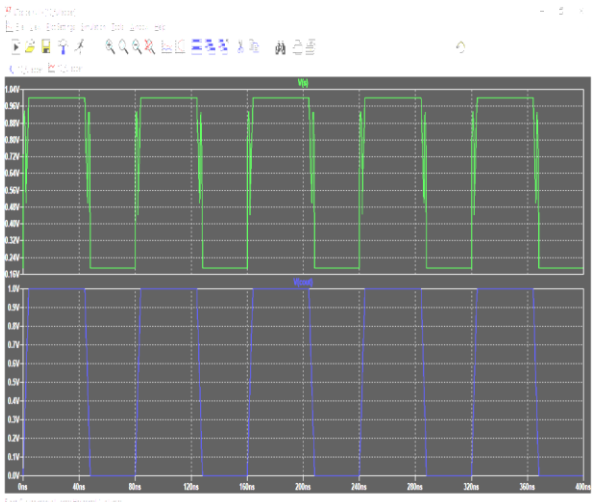

Fig.4 output of the PTL based 14T full adder

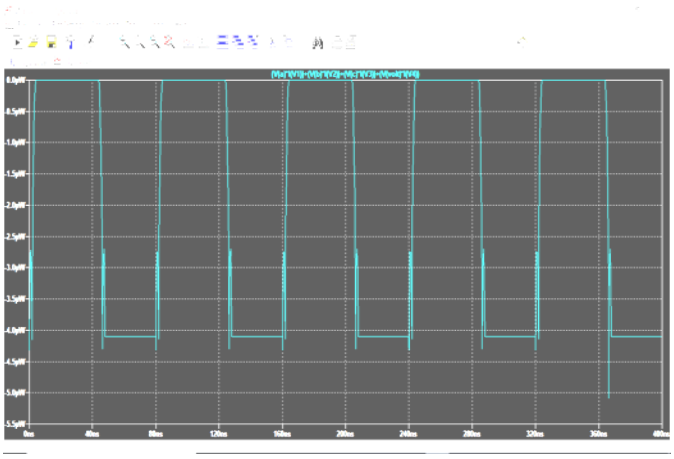

Fig .5 power of the PTL based 14T full adder

To pursue with lower transistors count full adder designs, pass transistor logic (PTL) can be used. In [9] PTL based XOR function is used for the implementation of 14 transistors full adder circuit as shown in Fig. 4. This design also provides full swing output voltage but suffers from high power consumption due to the inverter required for getting XNOR function out of XOR. Another PTL based adder, SERF is presented in [10]. It uses only 10 transistors but has the problem of threshold loss.

$$SUM = A \oplus B \oplus C$$

$$CARRY = (B \oplus C)A + BC$$

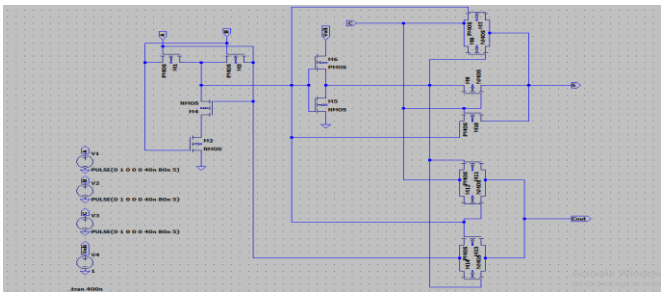

Fig . 6 simulation circuit PTL based 14T full adder

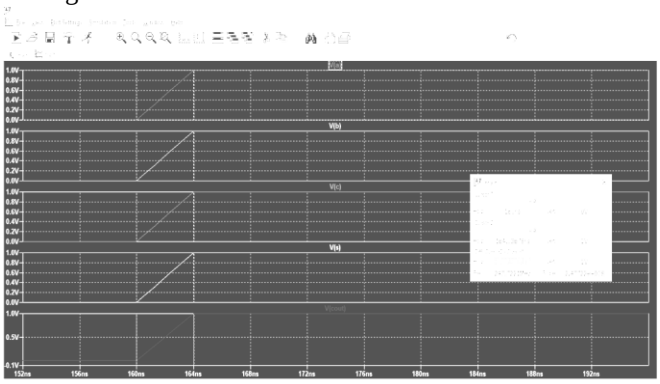

Fig .7 Delay of PTL based 14T full adder

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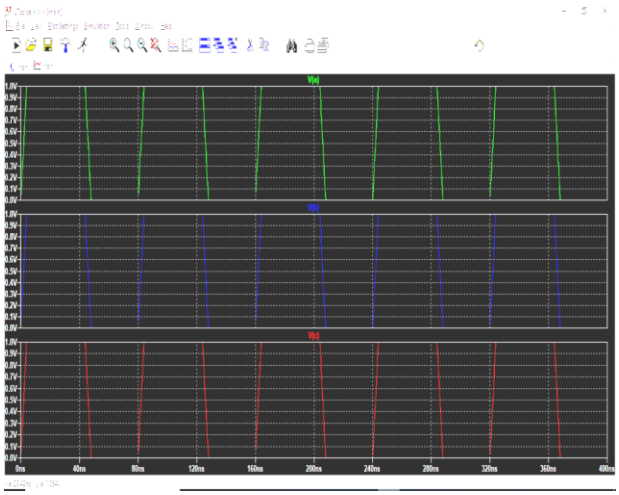

Fig. 8 Input of PTL based 14T full adder OUTPUT.

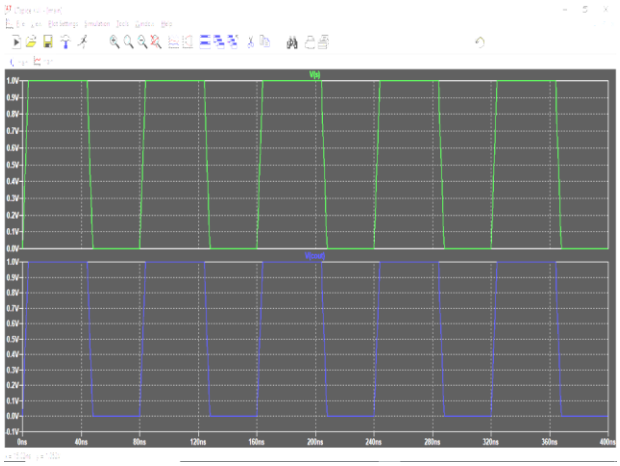

Fig . 9 Output of PTL based 14T full adder

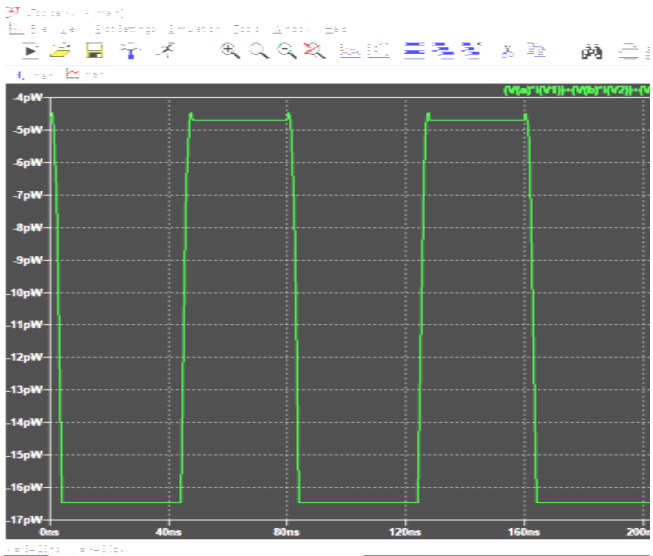

Fig. 10 power of PTL based 14T full adder

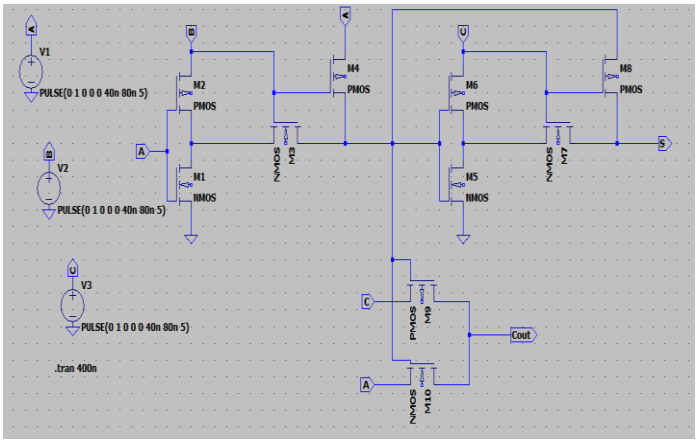

Fig . 11 simulation circuit 10 T full adder

A transmission gate based full adder design using 20 transistors was presented. This circuit can operate with full output voltage swing. These designs were further improved by using only 14 transistors while maintaining the full output voltage swing operation. a 10-transistor full adder reported with full swing. It employs PTL along with the invertors to eliminate the threshold loss problem. However, the addition of invertors induce short-circuit power loss.

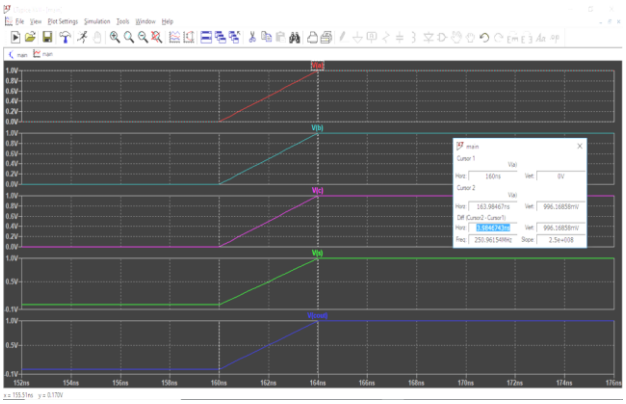

Fig. 12 Delay of PTL based 10T full adder.

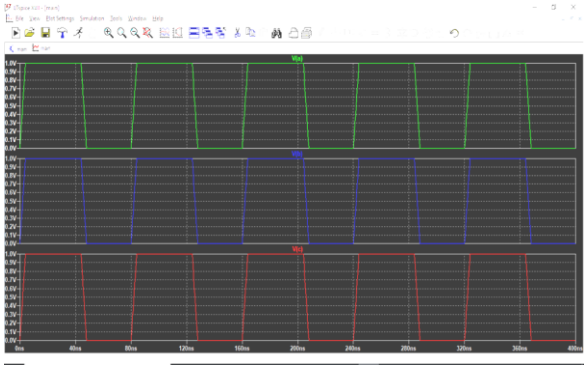

Fig. 13 input of PTL based 10T full adder

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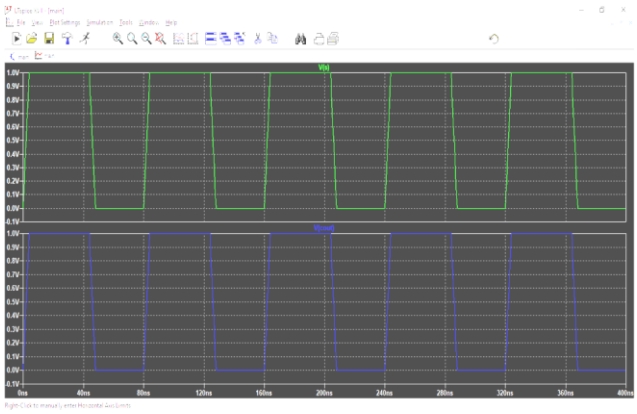

Fig. 14 Output Of PTL Based 10T full adder.

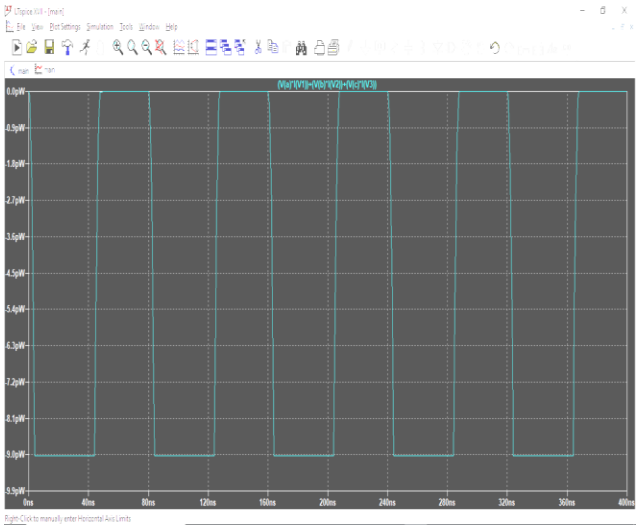

Fig. 15 power 10T full adder

14T

To pursue with lower transistors count full adder designs, pass transistor logic (PTL) can be used. In PTL based XOR function is used for the implementation of 14 transistors full adder circuit as shown in Fig. 4. This design also provides full swing output voltage but suffers from high power consumption due to the inverter required for getting XNOR function out of XOR. Another PTL based adder, It uses only 10 transistors but has the problem of threshold loss. Proposed and reference full adders designed at layout are simulated LTSPICE, power consumption and logic level at the nodes SUM and CARRY results for Vdd=1V are collected and analyzed.

The high logic in the reference adder circuit is degraded due to two series connected on NMOS pass transistors when all the inputs are high whereas in the proposed circuit, SUM is always at strong high logic due to inverter in the path. This arrangement in the proposed adder circuit also reduces voltage drop at the SUM node which saves considerably dynamic power consumption. The high logic at the CARRY node degraded in the reference circuit, when all inputs are high, due to two series connected on transistors whereas in the proposed adder circuit carry maintains its high logic. When all the inputs are low, there are only two series connected NMOS transistors in sum path of the proposed circuit whereas in reference circuit one inverter is added in between two transistors which degrades the access time and increase the total parasitic capacitance. The proposed circuit faces the same problem in the carry path.

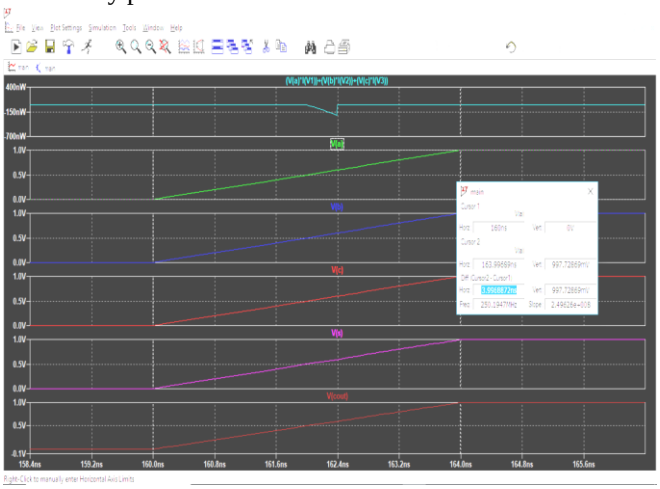

Fig 16 Delay 10T Full Adder

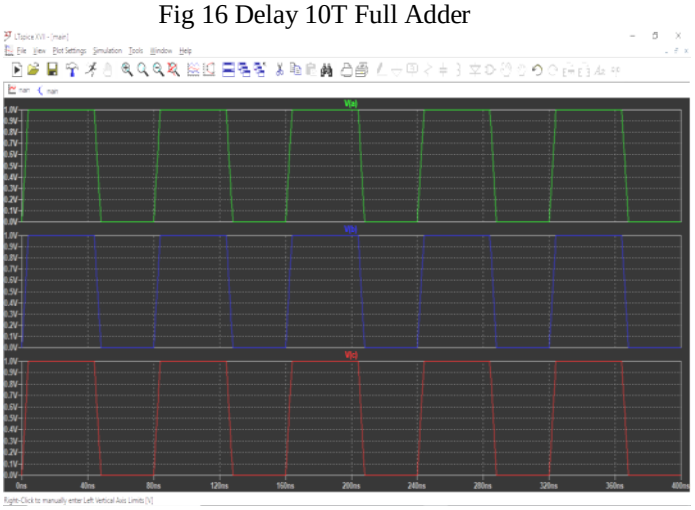

Fig 17 Input 10T Full Adder

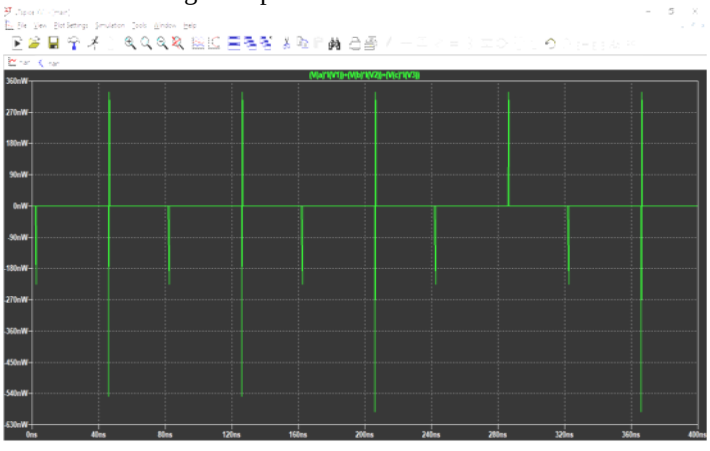

Fig 18 Power 10T Full Adder

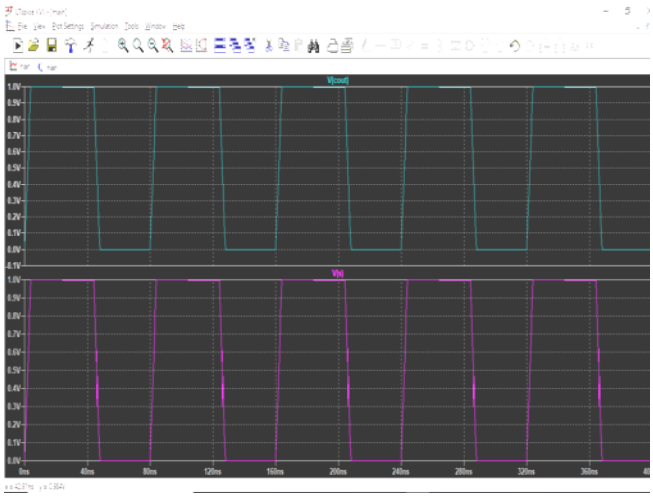

Fig. 19 output 10T full adder

IV. CONCLUSION

For simulation on in different-different technique and circuit parameter in lOT Adder cell and result that the lOT Adder is the most prominent low power consumption cell. The leakage power can be reduced by using various techniques. We have found that VT is the most appropriate parameter for leakage power and current Simplification of Boolean expression and the arrangement of the transistors and inverters are important in maintaining high logical level for both sum and carry and to recover power consumptions; dynamic power and static power. It is observed that proposed PTL adder circuit is stable, reliable and power efficient due to lower parasitic capacitance and resistance. The proposed circuit suffers less logic degradation due to less number of gates required to implement the CARRY.

Future Research Directions Due to the inherent tradeoff between different performance metrics of CMOS circuits and specially the ultra reduced size and low power consumption requirements has led investigate new technologies. Some of these technologies are Single Electron Transistors (SET), Quantum Dot Cellular automata (QCA), Multi Gate Field Effect Transistor (MUGFET) and Carbon Nanotube Field Effect Transistor (CNTFET). Among these technologies, CNTFET has been proven as an alternative for conventional MOSFET for the future VLSI circuits

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