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Adiabatic Logic Circuits Designfor Low Power in Applications in Digital Circuits

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Abstract- With the continuous scaling down of device technology in the field of VLSI circuit design, low power dissipation has become one of the primary concern of the research field. With the increasing demand of low power portable devices, adiabatic logic gates prove to be an effective solution. This paper presents different types of adiabatic logic families such as 2N-2N2P, PFAL (Positive Feedback Adiabatic Logic), DCPAL (Differential Cascode and Pre-resolved Adiabatic Logic) and a proposed circuit based on the PFAL logic circuit. This paper investigates different adiabatic logic families such as ECRL, 2N-2N2P and PFAL. All simulations are carried out using HSPICE at 65nm technology with supply voltage is 1V at 100MHz frequency, for fair comparison of results W/L ratio of all the circuit is same. Finally average power dissipation characteristics are plotted with the help of a graph and comparisons are made between different logic families.

Keywords- Low power, Adiabatic logic, ECRL, 2N-2N2P, PFAL.

I. INTRODUCTION

If there is need to design a circuit for low-power consumption for low power consumption application then it is important to have a thorough understanding of the sources of power dissipation, the factors which affect them, the methodologies and techniques that are available to achieve optimal results.

Therefore, my thesis starts with the sources of power dissipation. Power consumption is composed of two parts: dynamic power and static power. The dynamic power is due to the switching activities during charging and discharging process, while static power is caused by the device internal leakage when the circuit is in the idle state [1].

Therefore, both dynamic power and static power need to be studied in the low-power VLSI circuit design. Low-power design can be applied on different levels, such as the architectural level, the gate level, and the technology level. A lot of novel circuit technologies like sub-threshold circuit [2] and multi-threshold technology [3] has been introduced to reduce dynamic power. Losses due to leakage currents are in focus with on-going shrinking of electronic circuits. Power-gating does not supply power to the circuits in off state from the power supply.

Non-critical paths within a complex system can be equipped with higher V_th devices, results in a trade-off of speed for passive losses.

Apart from these circuit level methods to reduce leakage losses also new transistor models are presented to minimize leakage losses in circuits.

Adiabatic Logic technique is one of the best circuit design methods to reduce energy consumption in different operations. Analysis of adiabatic logic on the gate level suggests a major cut-down of losses compared to static CMOS. Adiabatic logic utilizes AC voltage supply rather than DC voltage supply to recycle the energy of circuits.

This method forces the node voltage to vary synchronously with the power supply; as a result, the energy stored in the node capacitance is only 0.5 CV_{DD}^2, which avoids the heat dissipation in charging and discharging period. Furthermore, the energy stored can flow back to the voltage supply when the supply recovers to zero. Theoretically, zero power consumption can be realized by the adiabatic logic without considering the leakage power. [10-15].

In this paper, power dissipation is calculated for different logic gates using different adiabatic logic circuits and results are compared to see the effectiveness of different adiabatic logic families as compared to conventional CMOS circuits.

The rest of the paper is organized as follows: Section 2 overviews the conventional CMOS and adiabatic logic circuits. In section 3, simulation of circuits is done and results of power dissipation are compared. The paper ends with the conclusion given in section 4.

II. CONVENTIONAL CMOS AND ADIABATIC LOGIC

The previous section has been explained about the conventional CMOS power consumption, where the major power dissipation is dominated by dynamic power (charging power).

A lot of circuit technologies like multi-threshold technology [3] and sub-threshold circuits [2] have been introduced to reduce the dynamic power. In this section, the adiabatic logic principle is adopted to lower the peak supply current for resistance [23]. Adiabatic switching is commonly used to minimize energy loss during charging / discharging.

The term 'adiabatic' comes from 'thermodynamics', which describes a process wherein, no exchange of energy with the environment take place, so no energy loss due to dissipation occurs. Whereas in semiconductor devices, the charge transfers between different nodes is the process of energy exchange. So, different techniques can be utilized to minimize this energy loss due to charge transfer.

While fully adiabatic operation would be the ideal condition of a circuit operation, in practical cases partial adiabatic operation of circuit gives acceptable performance without much complexity.

The principle behind adiabatic switching is that, the transitions should be sufficiently slow so that heat is not emitted significantly. This is achieved by using AC power supply rather DC power supply to initially charge the circuit during specific adiabatic phases and then dischargethe circuit to recover the supplied charge.

Due to this the node voltage vary synchronously with the power supply as a result, the energy stored in the node capacitance is only 0.5 CV^2, that avoids the heat dissipation in charging and discharging process. As it is known that, a constant charging current source that is a linear voltage ramp is used. If the constant current source delivers the charge ($Q = CV_{DD}$) during the time period T, the energy dissipated in the channel resistance R is given by

$$E = I^2RT = \left(\frac{CV_{DD}}{T}\right)^2 RT = \frac{RC}{T}CV_{DD}^2$$

Where, V_{DD} is supply voltage, R is resistance of MOSFET. *T* is time period of circuit is node capacitance. From equation (7), as the T is increased linearly, power dissipation will decrease. If T is made sufficiently larger than RC, the energy dissipation will be nearly zero. This is the principle of adiabatic switching.

Fig.4.1 (c) graph shown is the comparison of the peak current traces of the conventional CMOS logic and adiabatic logic using respective equivalent RC model. In this figure for CMOS, a large amount and sudden flow of current is observed as indicated with black line and a gradual increase of supply current peak can be seen in the same figure with red colour line. So by comparison, adiabatic circuit is showing low peak current than that of the CMOS peak current. As power consumption is a function of instantaneous supply current and voltage, therefore, as the total amount of current flow in the circuit is less in adiabatic circuit, the power dissipation will be definitely lower compared to the CMOS logic.

1. Adiabatic LOGIC:
The use of AC power clock as opposed to DC supply makes the adiabatic circuits capable of recovering the stored energy of node capacitors back to the power source, and hence, avoid the dynamic power loss almost completely, theoretically. The use of adiabatic logic principle in designing of low power circuits, is continuously growing, and is proving to be a better selection in comparison to other conventional circuits [Fig.1].

In the WAIT phase the power clock stays at low (zero) value, which maintains the outputs at low value, and the evaluation logic generates pre-evaluated results. Now, since the power clock is at low level, the pre-evaluated inputs will not affect the state of the gate. In the EVALUATE phase, the power supply ramps up from zero to Vdd gradually, and the outputs will be evaluated as per the result of pre-evaluation logic.

In the HOLD phase, power clock stays high, providing the constant input signal for the next stage in pipelining of adiabatic circuits, and keep the outputs valid for the entire phase. Meanwhile inputs ramp down to low value. In the RECOVERY phase of operation, the power supply ramps down to zero and the energy of the circuit nodes is recovered back to the power source instead of being dissipated as heat [12].

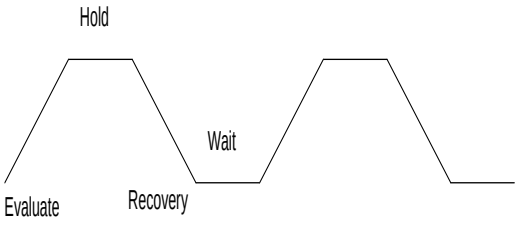

Fig 1. Four Phased Trapezoidal Power Clock.

2. Efficient Charge Recovery Logic (Ecrl):
Efficient Charge Recovery Logic (ECRL) [5], as shown in Fig. 2, uses two cross-coupled PMOS transistors and two NMOS transistors in the N-functional blocks of ECRL logic block. In order to recover and reutilize the supplied energy, ECRL gates uses AC power clock (pck). Let us assume **in** is at high and **Inb** is at low. At the beginning of

a cycle, when power clock 'pck' rises from zero to VDD, **Out** remains at low level because the high input **In** turns the F NMOS logic high. Output **Outb** follows the power clock 'pck' through M1. Now when 'pck' reaches to VDD, the outputs hold valid logic values. During the hold phase these output values are maintained and can be used as inputs for evaluation of next stage.

In the next phase of recovery, the power clock falls down to zero level and the energy from the output node can be returned to the 'pck' so as to recover the delivered charge [13-16].

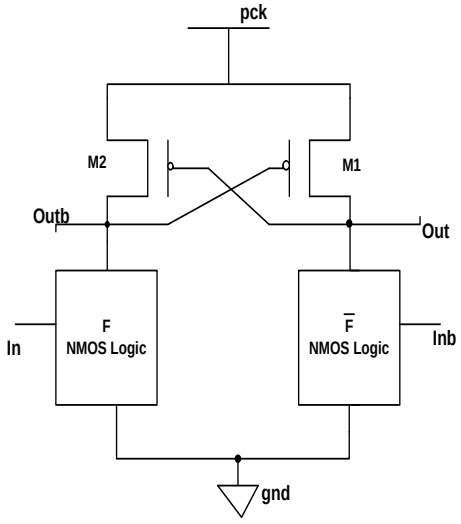

Fig 2. Efficient Charge Recovery Logic (ECRL).

3. 2N-2N2P Logic:

The most widely used adiabatic logics are 2N2P, 2N2N2P, PFAL and DCPAL. These four types' adiabatic buffers are discussed below. They have similar in operations with 2N2P logic but have some differences also.

In the 2N2N2P logic, the two more N-MOSFETs with P-MOSFETs make up two inverters to cross-couple that increases the stability of the outputs. The PFAL logic holds the evaluation logic upward to the pull-up blocks forming two charging paths with a pair of cross-coupled P-MOSFTEs, hence reduces the time taken to evaluate the outputs.

This structure can provide complete charge recovery by eliminating the charge stored in the output node after the recovery phase. In DCPAL a gating N-MOSFET is added in the pull-down path which helps in the suppression of leakage current.

So, considerable dynamic power reduction can be achieved by adiabatic circuit. However, with the aggressive scaling of devices technology, the leakage power becomes more and more dominant. Hence, leakage current should be carefully considered in the adiabatic circuit design.[10, 17-19].

4. Positive Feedback Adiabatic Logic (Pfal):

The Positive Feedback Adiabatic Logic (PFAL) achieves the lowest power consumption as opposed to other similar adiabatic logic families. The generalized PFAL circuit diagram is shown in Fig.4. The latch is made similar to the 2N-2N2P logic circuit with two PMOS transistors and two NMOS transistors.

The functional blocks of NMOS logic are connected in parallel with the PMOS transistorsof the latch and form the transmission gates. The fact that the functional blocks are in parallel with the PMOS transistors, the equivalent resistance is smaller during the charging of capacitance [13, 20-22].

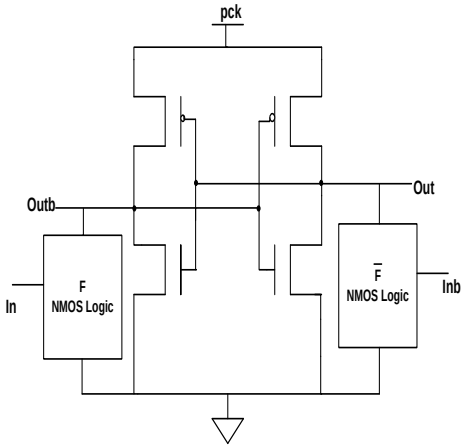

Fig 3. 2N-2N2P Basic Logic circuit.

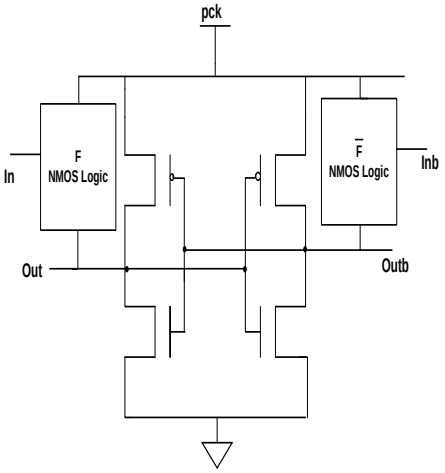

Fig 4. PFAL Basic logic circuit.

During the recovery process, power clock CLK goes down to 0. Charge at /OUT is at higher potential than the CLK, which flows back to CLK and hence /OUT starts to fall. The Wait Phase helps in resetting the present stage and waits for next evaluation stage. This cycle of operation repeats across the stages of the adiabatic pipeline.

Assuming input IN High, the device MN3 conducts and pulls the OUT node towards power clock, which in effect

makes MP2 to switch off and OUTB is disconnected from power clock. It may be noted that the pull up network resistance Ron decreases with the parallel path formed by MP1 and MN1.

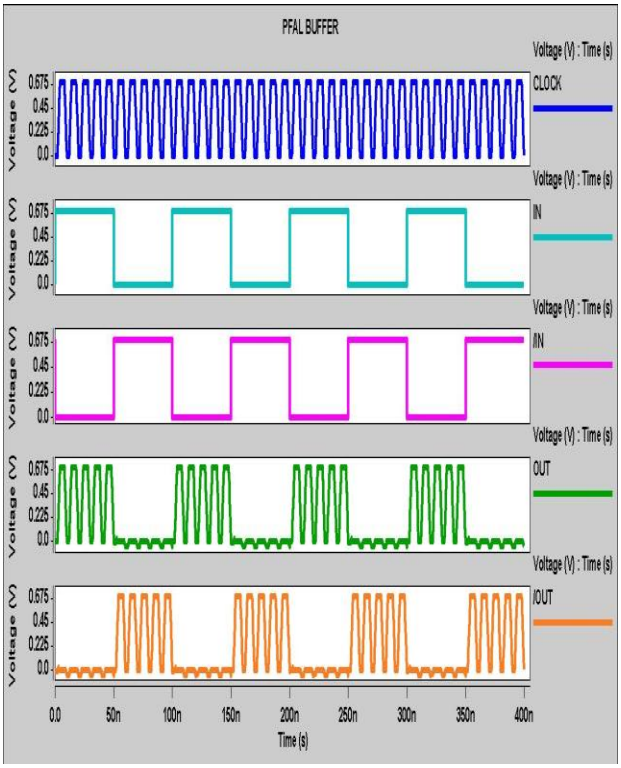

Fig 5. (a) Basic Structure of Two input PFAL BUFFER Logic (b) Simulated waveform of PFAL BUFFER Logic.

III. PROPOSED WORK

ON OFF DCDB-PFAL abbreviated as Diode Connected DC Biased-Positive Feedback Adiabatic Logic is an adiabatic logic circuit which is an enhanced version of Positive Feedback Adiabatic Logic (PFAL) family circuits. Fig 5.1 given below is the diagram of proposed adiabatic circuit design.

Proposed circuit is quite similar to PFAL adiabatic logic which comprises of two back to back inverter which form the latch of the circuit. And the NMOS logic functional blocks is parallel with the PMOS pull up transistors which form the latch, in transmission gates design.

The main fact is to reduce the transistor count with reduction of power consumption by making proper arrangement of the circuit.

- NMOS transistor forming a diode with its drain and gate shorted together is connected below the pull-down NMOS network.
- A DC Voltage is connected between PDN and ground of the circuit in order reduces the charge which improves the power of the circuit.

IV. SIMULATION AND RESULT

In order to see the effectiveness of different adiabatic logic families over conventional CMOS circuits, different logic gates have been implemented, first using conventional CMOS logic family and then by using the adiabatic principle of different adiabatic logic families as discussed in this paper and power calculations are made as shown in Table II.

The universal logic gates have been simulated using PFAL as well as ON OFF DCDB PFAL and the results have been analysed. Fig.6, Shows the comparison of all adiabatic circuit design.

Table 1. Design Parameters.

TYPE	CMOS	Adiabatic Logics
PMOS (width)	260 nm	260 nm
NMOS (width)	130 nm	130 nm
Power supply	1 V DC supply voltage	Trapezoidal power clock, 0v- 1v, frequency: 200MHz
		Rise Time: 1.25 ns, Fall Time: 1.25 ns

Table 2. Average Power Dissipation for Different Logic Devices.

Logic	Gate	Power (Nw)	Delay (Ps)	Pdp (Zj)	Edp E^ (-30)
PFAL	Inverter	0.3432	13.31	4.5680	0.0608
	Nor	0.6828	9.398	6.4170	0.0603
	Nand	0.6553	27.25	17.8569	0.4866
	Xnor	1.241	30.21	37.4906	1.1326
DCDB-PFAL CKT	Inv	0.281	12.57	3.5322	0.0035
	Nor	0.5054	8.196	4.1422584	0.0041
	Nand	0.4551	29.43	13.393593	0.0134
	Xnor	0.9634	36.51	35.173734	0.0352

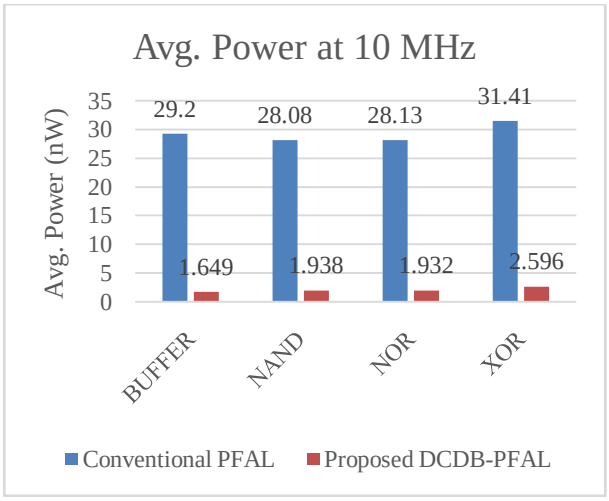

Fig 6. Average power comparison of conventional PFAL vs. proposed DCDB-PFAL basic gates at 10MHZ at 32nm.

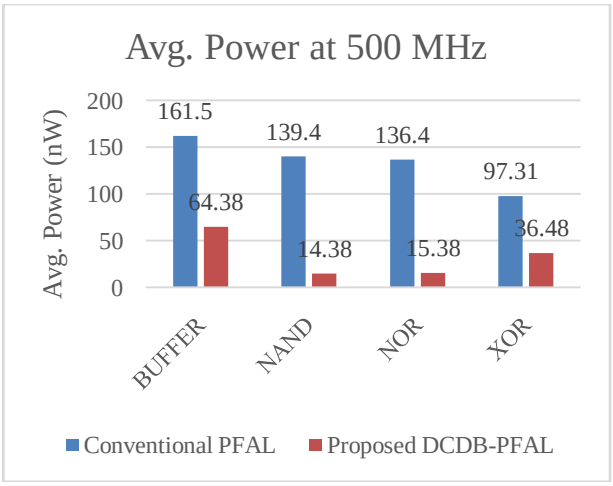

Fig 7. Average power comparison of conventional PFAL vs. proposed DCDB-PFAL basic gates at 500 MHz at 32nm.

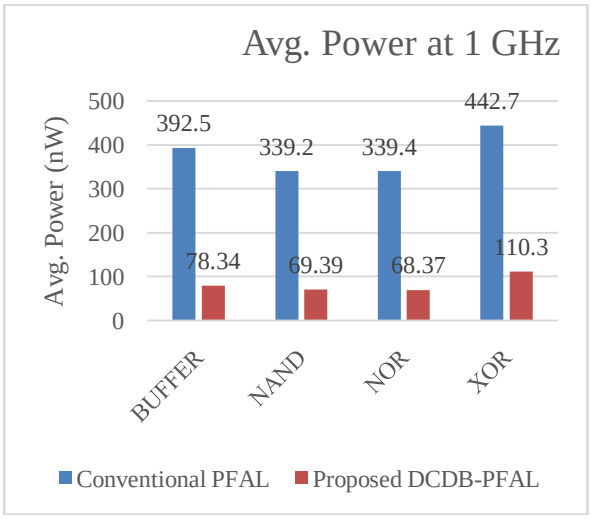

Fig 8. Average power comparison of conventional PFAL vs. proposed DCDB-PFAL basic gates at 1 GHz at 32 nm.

V. CONCLUSION

This paper reviews the adiabatic logic circuits and some important adiabatic logic families have been described and compared for their effectiveness in terms of reduced power dissipation as compared to conventional CMOS logic circuits observed that adiabatic logic designs are quite better than the CMOS logic designs in terms of power consumption which all mostly half than CMOS design by applying trapezoidal pulse saves the power consumption in adiabatic circuit design.

The adiabatic logic save the power in dynamic condition mainly it reduces the switching activity of the circuit i.e. there charging and discharging time of the load capacitance is almost reduces, it slowly charge and discharge the transistor. As the quest for ultra-low power circuit designs keeps on increasing, these improved circuit technologies would prove to be very useful in serving the need.

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