International Journal of Scientific Research & Engineering Trends
Volume 7, Issue 4, July-Aug-2021, ISSN (Online): 2395-566X

Low Power Adiabatic Logic Design for VLSI Applications

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***Abstract*- The ever-increasing transistor integration in VLSI have augmented the power dissipation due to transistor switching in a massive amount. Power reduction and low power circuits have become a major research topic now a days. Adiabatic logic style is found to be an effective solution in achieving low power. In this paper, various adiabatic logic approaches have studied and compared with a proposed adiabatic logic based on PFAL logic circuit. Adiabatic logic styles such as 2N-2P, 2N2N-2P, DCPAL and PFAL are considered and their average power dissipation and delay at different frequencies are compared with the proposed circuit. the proposed circuit has achieved the average power consumption of 1.649nw, 1.938nw, 1.932nw, 2.596nw for BUFFER, NAND, NOR and XOR circuits respectively at 10MHz. At 32nm technology the average power consumption of 0.842nw, 0.942nw, 0.957nw, 1.038nw for the same logic at 10 MHz. From the results it is concluded that proposed ON OFF DCDB-PFAL based circuit performed very well and achieved lowest power consumption among all other adiabatic logic circuits.**

***Keywords*- Adiabatic Logic, Low power, 2N2P, 2N2N2P, DCPAL, PFAL, Modified PFAL, Switching dissipation.**

I. INTRODUCTION

In recent years, there is a huge demand for low power and high speed digital circuits designed by VLSI (Very Large Scale Integration). Designers are introducing new methods to the design of low power VLSI circuits. In general, power reduction can be done at different levels of design abstraction: system, circuit, architectural, gate and the technology level. Various approaches are available for designers looking to reduce power consumption, by means of minimizing supply voltage, switching capacitance, switching activity, leakage power and using static and dynamic power reduction techniques. These techniques are not sufficient enough to meet today's power requirement.

The ceaseless need for low-power circuits is now motivating designers to explore new options in circuit designs. A need for low power VLSI circuit design arises from evolution of low power portable devices based on integrated circuits. While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size of the integrated circuits, reported by Chandrakasan et al (1999). Now the adiabatic logic is effective approach to offer a possible solution to low power circuit design. Thus, by using adiabatic technology low power ON OFF DCDB-PFAL adiabatic logic circuit has been designed.

Adiabatic logic is accomplished through keeping less potential across the switching devices, for that, load capacitor is charged from a time varying voltage source (AC) or a constant current source only. Basically, there are two types of adiabatic circuits, Fully adiabatic and partially adiabatic or quasi adiabatic circuits. Fully adiabatic circuits provide zero wastage of energy i.e. it does not have any non-adiabatic loss. But it is more complex to design than quasi adiabatic circuits and it also have problem with operating speed and synchronization of power clock of the circuit. Several adiabatic logics have been proposed in literature over these years [2] [3] [4] [11].

The energy dissipated in these adiabatic logic circuits are significantly low while comparing with static CMOS circuits. So, the adiabatic logic circuits are promising contender for low power applications. To reuse the energy of circuit nodes, adiabatic logic circuits are sourced by AC power clock. In the circuit nodes, instead of the charge flowing to ground while discharging its flown back to the AC source. Thus, unwanted loss of energy on load capacitance due to discharging is restricted.

This paper analyzes various adiabatic logics styles like 2N2P, 2N2N2P, Differential Cascode Pre-resolve Adiabatic Logic (DCPAL) and Positive Feedback Adiabatic Logic (PFAL) and a proposed modified circuit of PFAL.

Four gates, INVERTER, NOR, NAND and XNOR are made with each logic and power and delay is obtained for different frequencies. The results are compared graphically with Power Delay Product (PDP) obtained in each case.

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Remaining portion of this paper is arranged as follows. Section 2 gives a brief study of conventional and adiabatic switching. Section 3 discusses working of different adiabatic logic styles. Proposed circuit is presented and discussed in section 4. In section 5 results of PDP obtained through various simulations are shown and compared through bar graphs. At last section 4 provides the conclusion of this proposed work.

II. BACKGROUND

1. Conventional CMOS:

Power dissipation in a conventional CMOS occurs mainly during the device switching time. A basic CMOS inverter is taken for explaining the energy dissipation. We can model PMOS and NMOS in the inverter as a resistor in series with an ideal switch for representing the channel resistance and interconnect resistance. The PMOS and NMOS are connected to a Load capacitance C_L due to the capacitance at the output node.

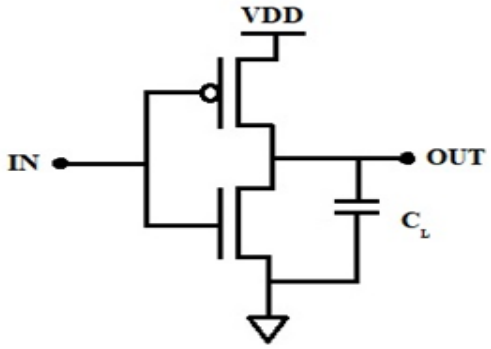

Fig 1. Basic CMOS Inverter.

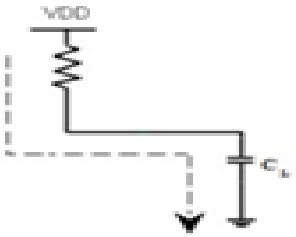

Fig 2. Charging of load capacitance.

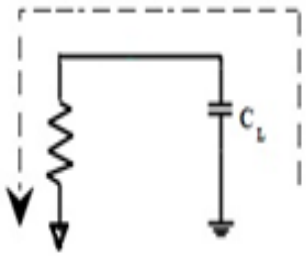

Fig 3. Discharging of load capacitance.

When a low level logic input is applied at the input IN there will be sudden discharge of current from the source through PMOS, which acts as a Resistor due to channel resistance [9][12]. The supply voltage will start to charge the load capacitance C_L through R as shown in Fig. 1. Power supply supplies a charge of $Q=C_L*V_{dd}$, hence the energy taken from the power supply will become $Q*V_{dd}=C_L*V^2_{dd}$. As we know the energy stored in a capacitor is always half that of energy supplied to it. The Energy stored in the capacitor will becomes,

$$E_{stored} = 0.5C_LV^2_{dd}$$

The rest half of energy supplied by power supply is dissipated in the PMOS resistance. Again, when NMOS become on, the charge stored in capacitance is discharged to the ground through NMOS resitance as in Fig. 3. For convenience, we have taken both PMOS and NMOS resistance as R. So, the total energy dissipated during a charging and discharging process in a conventional CMOS logic circuit is

$$E_{Total} = E_{Charge} + E_{Discharge}$$

$$=0.5C_LV^2_{dd} + 0.5C_LV^2_{dd} = C_LV^2_{dd}$$

From the above equation, it is clear that no energy is saved or recovered in conventional CMOS.

2. Adiabatic Logic

In fully adiabatic circuits, all charge on the load capacitance is recovered to the power supply. So, full-adiabatic circuits do not have adiabatic loss, but they are more complex than quasi-adiabatic circuits. Fully adiabatic circuits have some problems with respect to the operating speed and the power clock synchronization [6].

Full adiabatic methods are:

- Pass Transistor Adiabatic Logic (PAL)
- Split-Rail Charge Recovery Logic (SCRL)

2.1 Stages of Adiabatic Logic:

Adiabatic circuit operation consists of four phases [30] that is Wait, Evaluate, Hold and Recover. Quarter of period is the phase difference between adjacent phases. In Fig 4.3 (a) the adiabatic buffer structures are shown, that contain cross coupled P-MOSFETs and differential input N-MOSFETs. Also, time sequence of the adiabatic trapezoidal waveform depicting four phases is shown in Fig 4.3 (b) below.

Four operations of adiabatic logic are given below-

- **Wait:** Initially power supply stays at zero, the inputs become valid, the evaluation logic generates pre-evaluated result and output is at low voltage.
- **Evaluate:** Gradually, power supply rises from zero to, inputs remains stable and according to the result of pre-evaluation, output follows the power supply to become

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valid.

- **Hold:** The power supply remains high to keep the output valid and providing the constant input for the next stage in the adiabatic pipeline. Also inputs return to zero.
- **Recover:** The power supply return to zero. The zero input shut down the path to the ground, thus, charge stored in the node capacitance flow back to the power supply with the help of cross coupled P-MOSFETs.

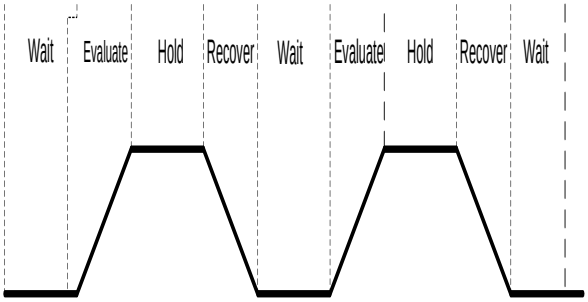

Fig 4. Four phases of trapezoidal waveform.

The most widely used adiabatic logics are 2N2P, 2N2N2P, PFAL and DCPAL. These four types' adiabatic buffers are discussed below. They have similar in operations with 2N2P logic but have some differences also. In the 2N2N2P logic, the two more N-MOSFETs with P-MOSFETs make up two inverters to cross-couple that increases the stability of the outputs. The PFAL logic holds the evaluation logic upward to the pull-up blocks forming two charging paths with a pair of cross-coupled P-MOSFTEs, hence reduces the time taken to evaluate the outputs.

This structure can provide complete charge recovery by eliminating the charge stored in the output node after the recovery phase. In DCPAL a gating N-MOSFET is added in the pull-down path which helps in the suppression of leakage current.

So, considerable dynamic power reduction can be achieved by adiabatic circuit. However, with the aggressive scaling of devices technology, the leakage power becomes more and more dominant. Hence, leakage current should be carefully considered in the adiabatic circuit design.

III. ADIABATIC LOGIC CIRCUITS

An adiabatic logic operates on one or more power clocks. Generally, a four phased trapezoidal power clock is used. Each phase signifies a particular stage of operation of an adiabatic circuit. The four stages of operation are Evaluate, Hold, Wait and Recovery as shown in the Fig. 4**.**

In the Evaluation phase, the outputs are evaluated with respect to input; the power clock rises towards V_{dd} from zero during this phase. The outputs are kept stable in the Hold state for providing the input for succeeding stages; power clock remains high during this phase.
After that the power clock starts to fall towards zero from V_{dd}, this phase is called recovery phase. The recovery of charge from load capacitor is taking place at this phase. A wait state is also inserted because it gives the power clock symmetry and generation of power clock become easier, also the input gets pre-evaluated at this phase.

1. 2N2P Logic:

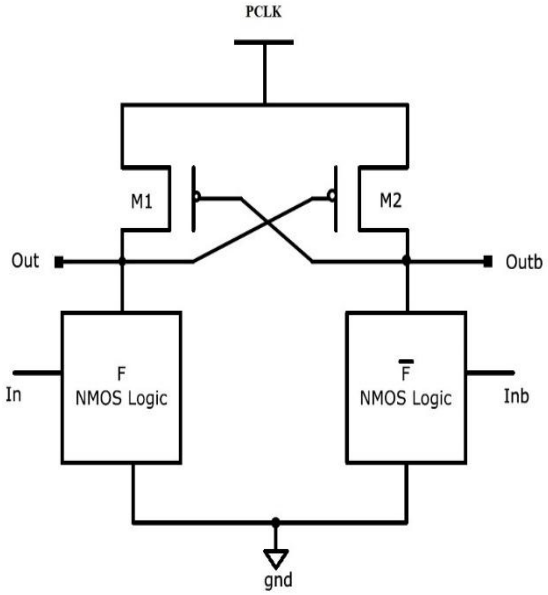

Fig 5. 2N2P Logic.

The 2N2P logic requires 2 N-mosfets for each input term and addition 2 P-mosfets as overhead for computation of digital operations. Based on this convention it's named as 2N2P logic. A basic 2N2P logic circuit is shown in Fig. 5. Differential logic is used in 2N2P logic; therefore, every logic will compute both the output and its compliment. Its one of the first adiabatic logic style came into the literature. Consider initially the inputs In and Inb are at logic high and logic low respectively and an AC source is applied at the power clock, let's say a trapezoidal clock.

At the beginning when the power clock starts to rise from zero to V_{dd}, the Out will get connected to the ground as the F-NMOS block is having a low resistance path to ground and this in turn switch on the PMOS M2 and it passes the power clock to the Outb. It results in setting Out at zero and outb will start to follow the power clock. Power clock reaches Vdd and stays there for some interval, i.e. Hold phase.

The hold phase keeps these output values stable and used as evaluation phase of subsequent stages. During the next phase, i.e recovery phase power clock falls down to zero and energy is recovered back by the power supply[11]. One of the major disadvantage of this circuit is the existence of coupling effect between the two PMOS latch.

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2. 2N-2N2P Logic:

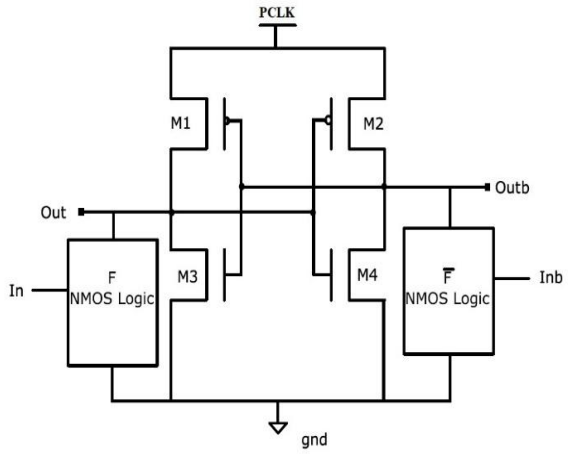

Fig 6. 2N-2N2P.

The 2N-2N2P is a variant of 2N-2P family; only difference is the 2N-2N2P uses an additional pair of NMOS which are cross coupled with each other. The structure of 2N-2N2P will be like a standard SRAM having a pair of cross coupled inverters as shown Fig. 6. The basic functioning of 2N-2N2P is similar to 2N-2P only. The added NMOS will reduce the coupling effects which were present in the former one.

It will also eliminate the floating node which was present in recovery phase of 2N-2P. Even though 2N-2N2P has these advantages the power consumption is little more due to added NMOS transistors in the structure.

3. DCPAL:

DCPAL, Differential Cascode and Pre-resolved Adiabatic Logic is a well-structured dual rail logic.Fig. 7shows the structure of DCPAL, which is similar to 2N-2P except a footer transistor is added and an extra power clock is used at its gate terminal. The power clock PCLK and PCLKb are inverted with each other. PCLKb is used for pre-resolving the inputs [4].

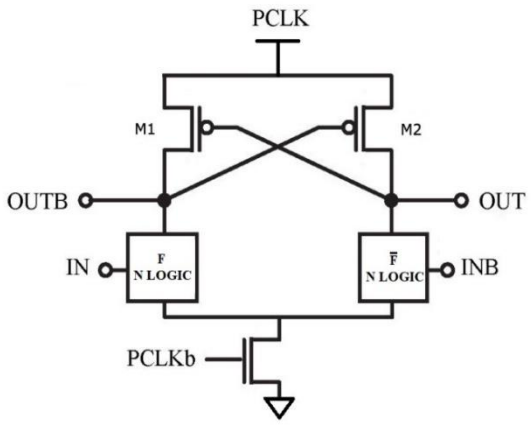

Fig 7. DCPAL.

When the PCLK is zero the footer transistor N3 will be ON as PCLKb is inverted, thus the leakage current due to power clock is controlled by N3 transistor and consumption is minimized. High energy recovery is possible in DCPAL in comparison with 2N-2N2P.

4. PFAL:

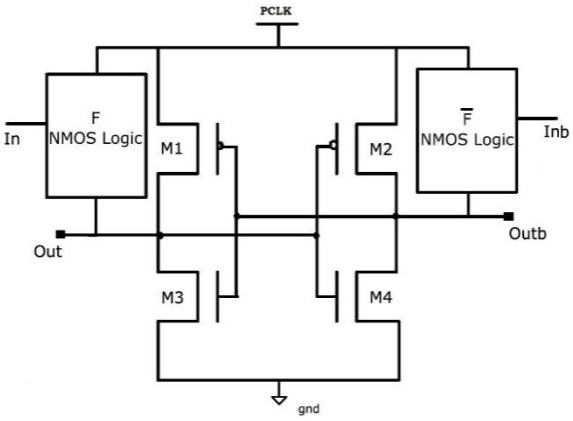

Fig 8. PFAL.

Postive Feedback Adiabatic Logic is operated with a four phased power clock. PFAL also have a latch element formed with two cross coupled inverters similar to 2N-2N2P. The basic difference between these two are, in PFAL the functional N block is in parallel with PMOS and in 2N-2N2P functional block is situated in the lower part parallel with NMOS. Fig. 8 shows a general PFAL logic. As every family described until now uses the same functional block and power clock, working is more or less alike.

The advantage of PFAL among others is it consumes less power when compared to others. As the functional blocks are in parallel with the transmission PMOS, the equivalent resistance of the charging path is comparatively smaller when node capacitance is getting charged.

IV. PROPOSED WORK

Figure 9 shows a generalized logic for the proposed circuit. This circuit is a modification of Positive Feedback Adiabatic Logic. So the structure is similar to PFAL, a cross coupled inverter is used for latching the output and the N-MOSFET based functional blocks are placed in the upper part which is in parallel with the PMOS transistors. This will form transmission gates at the upper part and reduce the effective resistance on charging time.

The difference lies in the lower part where an additional power clock is used and an extra NMOS and PMOS are implemented. The drain and gate of NMOS are shorted together, which makes it act as a diode. This diode will act as an active load and provides a high impedance discharging path.

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It will lead to decrease in the rate of discharging of the charge stored in node capacitance. A PMOS and a power clock for gating the PMOS is also used. The power clock PCLK2 is inverted and have double the frequency of original PCLK. The PMOS transistor is switched on for only a less time of the complete cycle; this will reduce the discharging time and thus allowing only less power dissipation.

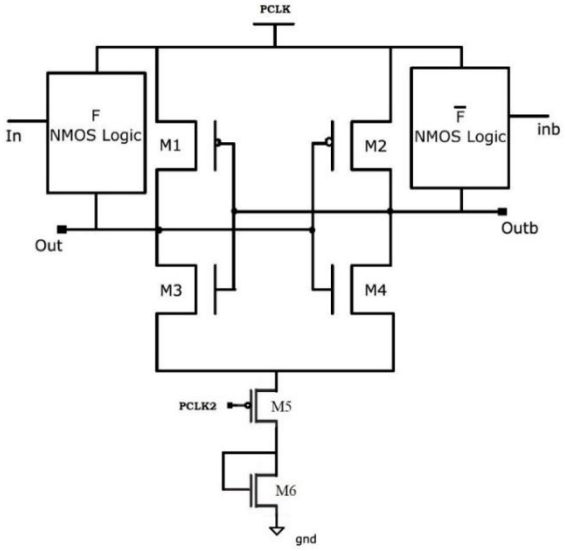

Fig 9. Proposed Work.

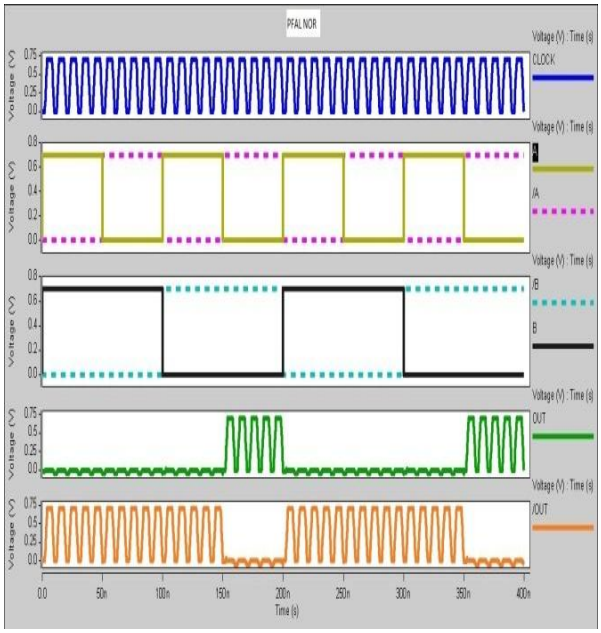

Fig 10. Output waveform of Proposed Circuit.

V. RESULTS AND DISCUSSION

Adiabatic logic circuits like 2N-2P, 2N-2N2P, DCPAL and PFAL where taken for analyzing the efficiency of the proposed circuit. Different logic gates of INVERTER, NAND, NOR and XNOR has been implemented with each adiabatic logic.

Each of them is simulated in frequencies of 10MHz, 100MHz, 500MHz and 1000 MHz's. Finally, all these logic gates are implemented in the proposed logic and results are compared with others. All the simulations are done in Cadence Virtuoso 65nm technology.

Table 1 shows the design parameters used in this paper. From Table 2,3,4,5 we can tell that 2N-2N2P dissipates more power comparing to others. It's because of the extra two NMOS at pull down network, which is used for avoiding the coupling effects. DCPAL shows better results than 2N-2N2P but the problem of coupling effect still exists in DCPAL.

After DCPAL, 2N2P logic style dissipates less power and has less delay. As in the literature PFAL confirms to be better than other adiabatic logic compared in this paper.

Table 1. Design Parameters.

TYPE	PFAL	PROPOSED
PMOS(Width)	180nm	180nm
NMOS(width)	90nm	90nm
Power Clock PCLK & PCLKb	1V Trapezoidal Power Clock, $f_{pclkb} = 2.f_{pclk}$	
Frequency	10MHz, 100Mhz, 500MHz, 1000MHz	

Table 2. Performance comparison with the proposed work at 10 MHz frequency.

Logic	Gate	Power (Nw)	Delay (Ps)	Pdp (Zj)
2N2N2P	INVERTER	2.174	103.4	224.7916
	NOR	2.049	107.6	220.4724
	NAND	2.512	146.4	367.7568
	XNOR	3.894	238.8	929.8872
DCPAL	INVERTER	1.355	35.75	48.4413
	NOR	1.45	37.35	54.1575
	NAND	1.748	54.64	95.5107
	XNOR	3.053	128.3	391.6999
2N2P	INVERTER	1.164	35.98	41.8807
	NOR	1.279	37.44	47.8858
	NAND	1.579	54.92	86.7187
	XNOR	2.747	144.6	397.2162
PFAL	INVERTER	.3432	13.31	4.5680
	NOR	.6828	9.398	6.4170
	NAND	.6553	27.25	17.8569
	XNOR	1.241	30.21	37.4906
PROP CKT	INV	.281	12.57	3.5322
	NOR	.5054	8.196	4.1423
	NAND	.4551	27.13	12.3469
	XNOR	.9634	30.17	29.0658

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Table 3. Performance comparison with the proposed work at 100 MHz.

Logic	Gate	Power (nW)	Delay (ps)	Pdp (Aj)
2N2N2P	INVERTER	50.9	113.9	5.7975
	NOR	42.99	115.9	4.9825
	NAND	52.55	130.1	6.8368
	XNOR	71.79	140.9	10.1152
DCPAL	INVERTER	25.12	85.02	2.1357
	NOR	25.64	87.77	2.2504
	NAND	32.28	105.4	3.4023
	XNOR	51.38	124.3	6.3865
2N2P	INVERTER	24.41	85.74	2.0929
	NOR	24.41	88.52	2.1608
	NAND	31.21	105.5	3.2927
	XNOR	48.69	121.1	5.8964
PFAL	INVERTER	8.208	15.88	0.1303
	NOR	12.65	9.828	0.1243
	NAND	12.7	28.93	0.3674
	XNOR	25.82	37.53	0.9690
PROP CKT	INV	8.176	11.41	0.0933
	NOR	13.16	7.609	0.1001
	NAND	11.27	24.56	0.2768
	XNOR	25.62	26.76	0.6856

Table 4. Performance comparison with the proposed work at 500 MHz.

Logic	Gate	Power (Nw)	Delay (Ps)	Pdp (Aj)
2N2N2P	INVERTER	529.8	48.65	25.7748
	NOR	416.6	49.44	20.5967
	NAND	465.2	58.43	27.1816
	XNOR	606.4	56.65	34.3526
DCPAL	INVERTER	275.6	40.92	11.2776
	NOR	259	41.81	10.8288
	NAND	291.1	51.2	14.9043
	XNOR	415.1	53.08	22.0335
2N2P	INVERTER	273.5	40.27	11.0138
	NOR	253	41.7	10.5501
	NAND	286	50.9	14.5574
	XNOR	661.8	49.97	33.0701
PFAL	INVERTER	148	14.13	2.0912
	NOR	199.2	7.827	1.5591
	NAND	198	21.3	4.2174
	XNOR	379.8	30.18	11.4624
PROP CKT	INV	127	9.982	1.2677
	NOR	193.3	6.651	1.2856
	NAND	178.7	18.3	3.2702
	XNOR	378.3	21.28	8.0502

Table 5. Performance comparison with the proposed work at 1000 MHz.

Logic	Gate	Power (nW)	Delay (ps)	Pdp
2N2N2P	INVERTER	1338	31.93	42.7223
	NOR	1027	32.22	33.0899
	NAND	1166	39.18	45.6839
	XNOR	1510	27.78	41.9478
DCPAL	INVERTER	683.9	27.42	18.7525
	NOR	628.6	27.63	17.3682
	NAND	714.8	35	25.0180
	XNOR	976.7	34.99	34.1747
2N2P	INVERTER	686.6	26.7	18.3322
	NOR	617.1	27.41	16.9147
	NAND	723.3	34.5	24.9539
	XNOR	993.2	32.76	32.5372
PFAL	INVERTER	512.4	13.44	6.8866
	NOR	648	7.295	4.7272
	NAND	648.6	17.57	11.3959
	XNOR	1161	27.78	32.2526
PROP CKT	INV	374.6	9.813	3.6759
	NOR	584.9	6.33	3.7024
	NAND	561.3	15.79	8.8629
	XNOR	1123	19.83	22.2691

Here from the Table 2, Table 3, Table 4, Table5 we can observe that all of the adiabatic logic circuits shows an increase in power as a factor of frequency. Unlike in CMOS logic, adiabatic logic shows a major disadvantage as variation of power proportional to the frequency.

CMOS logic circuits give a constant power on MHz frequency range. From the tables, we can also observe that DCPAL INVERTER gives up to 78% less Power Delay Product than 2N2N2P, 2N2P INVERTER gives up to 14% less PDP over DCPAL INVERTER and PFAL INVERTER gives a reduction up to 89% less than 2N2P INVERTER.

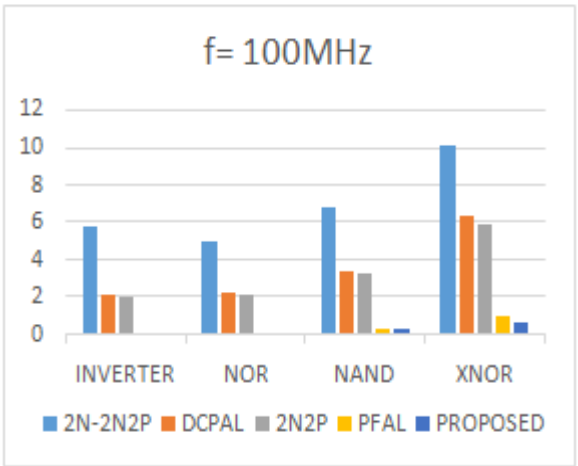

Fig 11. Power Delay Product comparison of PFAL and Proposed Logic at 100 MHz.

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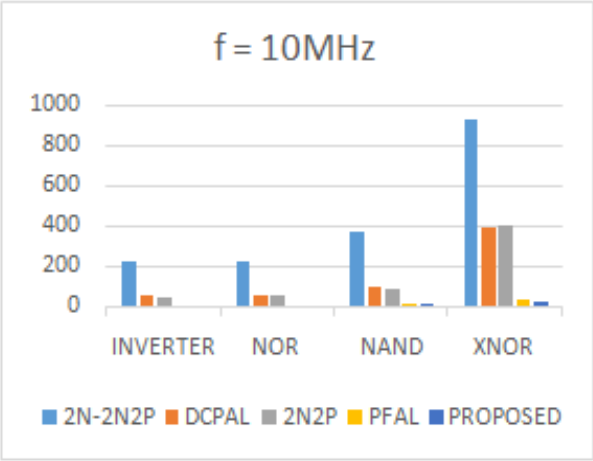

Fig 12. Power Delay Product comparison of PFAL and Proposed Logic at 10 MHz.

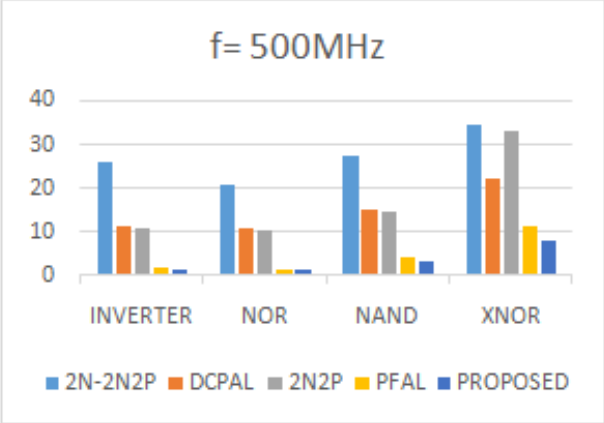

Fig 13. Power Delay Product comparison of PFAL and Proposed Logic at 500 MHz.

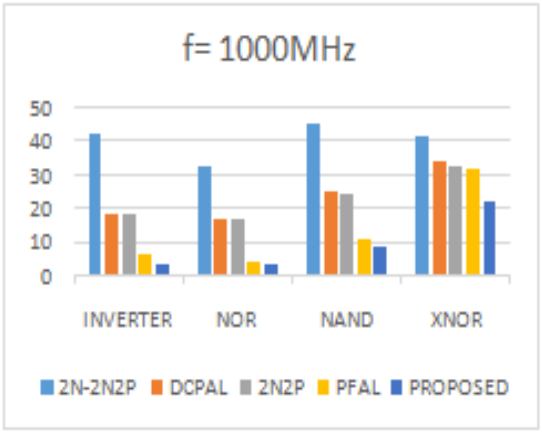

Fig 14. Power Delay Product comparison of PFAL and Proposed Logic at 1000 MHz

Proposed work shows significant decrease in power delay product. This is due to the added NMOS and PMOS. This extra circuitry increases the impedance of discharging path, which in turn will reduce the rate of discharging.

Also, clock given in PMOS is such that it allows discharging of node capacitor through PMOS happens only for less time. The results show that the PDP of proposed INVETER is 46% less than PFAL INVERTER.

The proposed NOR gate gives PDP upto 35% lesser than PFAL NOR. Neither proposed NOR gives up to 31% reduction in PDP while comparing to PFAL NOR and proposed XNOR gives up to 30 % lesser PDP than PFAL XNOR.

In all of the frequency range 10, 100, 500, 1000MHz the modified adiabatic logic confirms to be dissipating less power and gives better power delay product. It should be also noted that all of the adiabatic logic families analyzed here shows a deformation in output for higher frequencies above 300 MHz.

VI. CONCLUSION

In this paper, a review of some selected adiabatic logic styles is done. Different logic gates have been implemented on this adiabatic logic and proposed logic and simulated under various frequencies. The result of power delay product obtained shows a significant reduction in power. Comparing to PFAL adiabatic logic a reduction up to 46% in power delay product has been obtained. This Proposed work in adiabatic logic can be implemented in applications where ultra-low power consumption is required.

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