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Design and Implementation Low Power Consumption Level Shifter

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***Abstract*- A voltage level shifter is a circuit which converts low level input voltages to a desired higher level voltage or vice versa as desired, depending upon the system requirements. The major application of a voltage level shifter is in resolving mixed voltage incompatibility. The integrated circuits which are widely used nowadays may have different parts within, which operate at different voltage levels. Most of these circuits were provided with different supply voltage levels which prove to be difficult when the number of supply voltages increases within a single circuit increasing its complexity. Energy efficiency is a primary concern in modern CMOS circuits. Thus level shifters which are capable of converting a single low level voltage to other voltage levels have become useful in circuits having parts operating in multiple voltage domains. In the proposed design, the major aim is to lower the power dissipation and make the circuit faster.**

Keywords- Level shifter, sleepy keeper, power, delay, noise, voltage incompatibility.

I. INTRODUCTION

The growing market of mobile, battery- powered electronic systems (e.g., cellular phones, personal digital assistants, etc.) Demands the design of microelectronic circuits with low power dissipation. More generally, as density, size, and complexity of the chips continue to increases, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits.

In the past ten years, several techniques, methodologies and tools for designing low power circuits have been presented. However, only a few of them have found their way in current design flows [1].There are three major sources of power dissipation n in a CMOS circuit. Those are switching power, short circuit power and leakage power. Switching power is due to the charging and discharging capacitors driven by the circuit. Short circuit power is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously.

Finally, Leakage power is originates from substrate injection and sub threshold effects. One of the main reasons causing the leakage power increase is the increase of sub threshold leakage power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub threshold leakage power increase exponentially as threshold voltage decreases. Stack method, Forced NMOS, Forced PMOS and sleepy keeper method are the some of the leakage current reduction methods [2].

In the era of Complementary metal-oxide-semiconductor (CMOS) technology, low power consumption is one of the most key concerns to address in today's SoCs designs. The demand for low power and low output delay is very high, especially for handheld devices like cell phone, tablet etc. [1]. CMOS technology is being widely used to meet the increasing demand for low power consumption and low delay operation in microelectronics circuit systems [2] [3]. Considerable reduction in chip size (<1 mm2) has become possible with the advancement of CMOS technology which minimizes the manufacturing cost greatly. In multi-voltage systems, level shifter is a significant circuit component and usually used in between core circuit and input/output (I/O) circuit [4].

Level Shifters are used to convert the voltage level of an input signal to another voltage level at the output node. But the conventional level shifter dissipates high power and suffers from longer delay variation. Hence, the low power dissipation and low operation delay in level shifter have become major design issues for microelectronics circuits. Increases in power dissipation cause rise in reliability issues and limit the device portability [5] [6].

To meet the increasing demand for low power and high performance ICs, CMOS technology is being aggressively scaled [7]. The most effective way to minimize power dissipation in VLSI and other electronic circuit is to minimize their corresponding supply voltages. This is because of the quadratic dependence of the power dissipation on the supply voltage [2]. The delay variation occurs due to different current driving capabilities of transistors [8] [9]. The level

shifters are required to function appropriately when the difference between the two voltage levels is high. The high voltage difference may cause the failure of functionality in conventional LS circuit topologies due to low drive current when the supply voltage is very low [10] [11]. For the purpose of getting lower voltage from the high voltage domain, implementing CMOS inverters are normally adequate. But to get higher voltage from a low voltage supply domain in LS circuits, complicated circuit architectures are required. In order to design a simple LS circuit, proper design techniques must be utilized to balance the units of the circuit functioning at the high power supply voltage (VDDH) level with the input unit driving capability of the Level shifter [9] [1].

The differential cascade voltage switch (DCVS) topology described in figure 1 is considered as the traditional topology for LS circuit design. It comprises a half-latch composed of a pair of NMOS devices monitored by the differential low-voltage input signals A and AN and two PMOS transistors (MP2 and MP3). The topology acts as a ratioed circuit and there is a controversy between MN2 (MN3) and MP2 (MP3). As a result, to assure the accurate functionality proper balance must be maintained between the pull-down and pull-up strengths. In the CMOS circuit design, this requirement is very challenging to achieve when the input signals work around the threshold voltage levels [1] To face the current rising issues of LS design, different methods have been proposed by different researchers in the last few years. Zhai et al. have proposed an architecture based on four DCVS cascaded circuits which convert 200 mV to 1.2 V [4].

This architecture upgrades the voltage gradually having an interval of 0.01 V in each conversion stage and every conversion stage utilizes its respective VDDH. But this architecture required multiple numbers of power regulators to produce intermediate VDDHs which causes high power consumption. The LS solution suggested by Chen et al. [2] employed two PMOS current limiters in the conventional DCVS configuration. It minimizes the drive strength of the half-latch pull-up network. This design needs a reference path which should be kept "on" all the time for the current limiters to convert the sub-threshold input signals. It is considered as the main disadvantage of this architecture which is also responsible for greater static power dissipation. The Wooterset al. reported LS topology a single supply level shifter for low power and high speed applications composed of two stages [8]. The LS requires a fast delay to achieve a high performance. Even though various types of CMOS LS architecture are available, designers tend to use the simplest and easily integrable LS schemes.

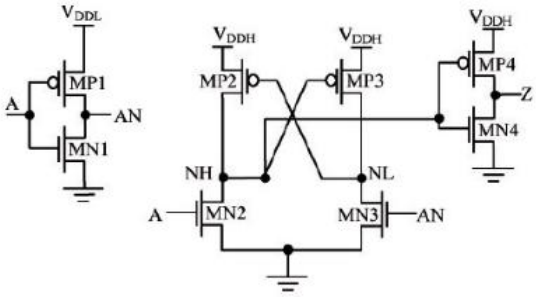


Fig. 1 Conventional DCVS level converter [16]

Therefore, the main challenge faced by the designers is to design a high-performance LS with simple LS architecture. To meet the demand of low power dissipation and low operation delay attributes, an improved LS design implemented in Silterra 0.13um CMOS process is presented in this article. The main challenge of designing an effective various-supply circuit is minimizing the cost of the level conversion between several voltage domains and at the same time keeping the total robustness of the design.1963 and pp. 118-132, Ap

II. LEVEL SHIFTER CIRCUITS

With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books etc., low power consumption has become major design consideration for VLSI circuits and system [1], [2]. With increase in power consumption, reliability problem also rises and cost of packaging goes high [3]. Power consumption in VLSI circuit consists of dynamic and static power consumption. Dynamic power has two components i.e. switching power due to the charging and discharging of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms [4].

The static power of CMOS circuits is determined by the leakage current through each transistor. Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance [4]. With the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage currents originate [5]. With the development of technology towards submicron region leakage power has become significant component of total power dissipation [6], [7]. Static power component of power consumption must be given due consideration if current trends of scaling of size and supply voltage need to be sustained.

In System on chip (SoC) design, different parts like digital, analog, passive component are fabricated on a single chip and needs different voltages to achieve optimum performance. Level converters are used to

convert the logic signal from one voltage level to other level and are the significant circuit component in VLSI systems. Level shifters are also important circuit component in multi voltage systems and have been used in between core circuits and I/O circuit.

Various design for level shifters have been reported in literature with single and dual supply [8] [6]. Conventional level shifter using 10 transistor with low voltage supply VddL and high voltage supply VddH has been reported [8], [10], [1], [2]. The conventional level shifters have disadvantages of delay variation due to different current driving capabilities of transistors, large power consumption and failure at low supply core voltage VddL[1]. The single supply level shifter allows communication between modules without adding any extra supply pin.

Single supply level shifters have advantages over dual supply in terms of pin count, congestion in routing and overall cost of the system. Another benefit of single supply is flexible placement and routing in physical design. Single supply level shifters dissipate higher leakage power due to increase in leakage currents when input supply level is lower or VddH is higher than input supply level by more than V_{tn}[12]. Contention mitigated level shifter (CMLS) using 12 transistors with reduced power consumption and delay than conventional level shifter has been reported [13]. Conventional level converters using bootstrapped gate drive to reduce voltage swings and power consumption has been reported [8]. In [14] method to modify the threshold voltage for reduce power consumption using dual supply voltage has been reported.

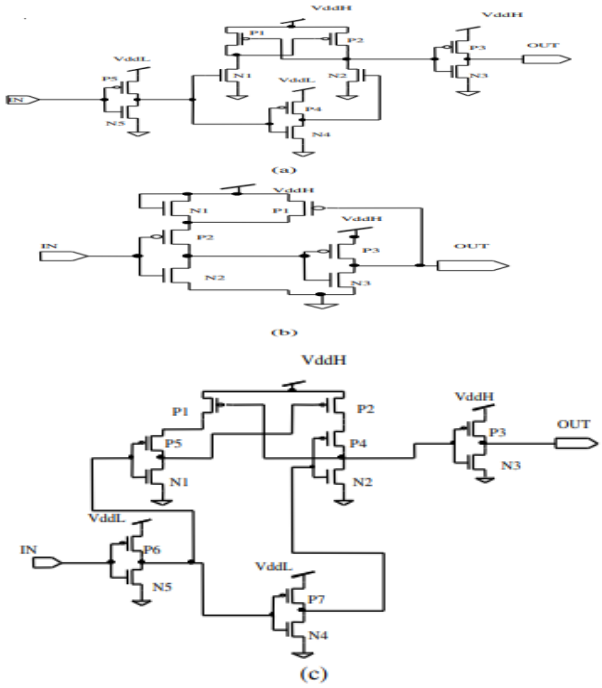


Figure.2. Level shifter circuits (a) Conventional (b) Single supply (c) Contention mitigated.

With increase in operating frequency and number of level shifters in data driver's circuits, power consumption has become major performance metrics. It has been reported that stacking of two off devices reduces the sub-threshold leakage as compared to single off device [7].

III. DYNAMIC VOLTAGE AND FREQUENCY SCALING (DVFS)

1. Introduction

Reducing power consumption is a major objective for almost any application [1]. Multiple supply voltages and dynamic voltage (and frequency) scaling (DVFS) are common techniques to achieve significant reduction in power with minimal overhead in performance [2], [3]. For both of these techniques, level shifters play an important role due to the signals that cross different voltage islands. When a low voltage signal is interfaced with a higher voltage domain, the voltage level should be increased with minimum overhead in power, area, and delay. The power consumed during level shifting reduces the overall power savings achieved by multiple supply voltages and DVFS. Furthermore, level shifters are also used in clock networks to achieve low swing clocking with significant power savings [4]–[6]. The delay of the level shifters is also important in this application since a larger delay increases the overall clock insertion delay, making the clock network more sensitive to variations.

Existing level shifters can be categorized under two primary classes: 1) shifters based on conventional, cross-coupled topology with differential output [7], [8], 2) shifters based on bootstrapping [9], [10]. Shifters in the first group enhance the delay of the level shifting by exploiting cross-coupled PMOS transistors whereas shifters in the second group enhance the power consumption by reducing the swing at the internal voltage nodes. In some applications where sub-threshold circuits are interfaced with super-threshold operation, wide range level shifters are required, as proposed in [8], [1]. Level shifters This research is supported in part by Semiconductor Research Corporation under Contract No.

2013-TJ-2449 and 2013-TJ-2450, and the Office of the Vice President for Research at Stony Brook University. With a single supply voltage have also been proposed [2]–[4]. However, shifting voltage swing with a single supply voltage typically produces large leakage current and long signal transition times.Power dissipation, especially leakage power, has become one of the most important design metrics in the deep submicron era. Dynamic Voltage Scaling (DVS) or VDD-hopping [1] is an effective technique that reduces not only dynamic power but also leakage power. A logic-swing level shifter is a key circuit component in the DVS implementation because even for a chip-level DVS system, I/O blocks are operated under fixed VDD and consequently level shifters are

required between core circuits and I/O circuits. When the VDD-hopping technique is applied on a "block level" as shown in Figure 1, each block on a chip could be operated under either high VDD (VDDH) or low VDD (VDDL). Thus, voltage level shifters are needed among blocks in order to avoid static crowbar current at a receiver side. Several level shifters have been proposed for use in I/O blocks [2] and in multi-VDD technology [3]. Since these level shifters have a contention problem, the delay and power at low voltage becomes larger and they are not suitable for use with VDDL. In this paper, the design of novel level shifters is described. The advantage of the proposed level shifters is verified by simulation and measurement.

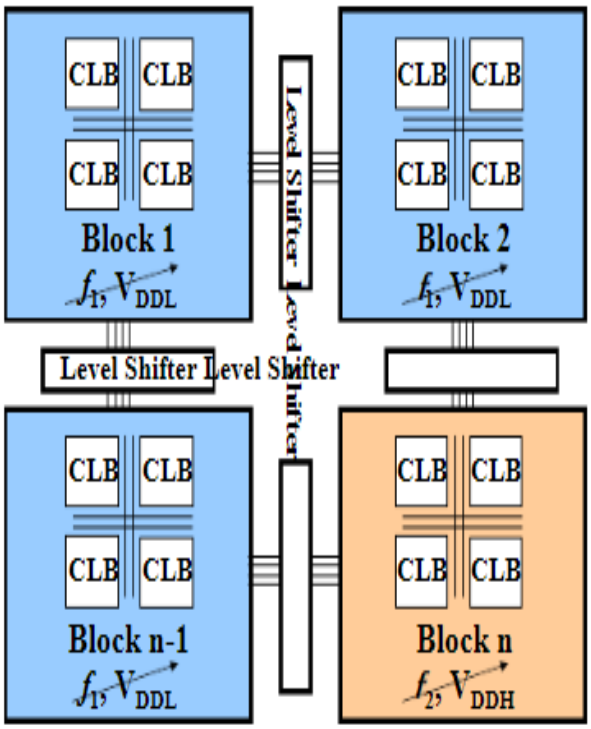


Figure 4 Block-level VDD-hopping.

3.2 Novel Level Shifter Design

The conventional level shifter is shown in Figure 2(a). The two PMOS transistors MP1 and MP2 act as a swing-restoring load. Assuming that initially input signal, IN, is "L", MN1 is turned on and provides a conducting path to ground while MN2 is cut off. Therefore, node A is pulled down to ground, which makes MP2 on and node B is pulled up to "H". Thus, the output signal, OUT, becomes "L". The operation reverses when the input signal, IN, is switched to "H". This conventional level shifter has large delay because it suffers from contention between the pull-down transistors (MN1 and MN2) and the pull-up transistors (MP1 and MP2). The contention problem gives rise to the increase in both delay and power consumption.

In particular, when the low voltage, VDDL, changes, the problem of contention gets severer because we can not get rid of the contention in both cases where VDDL is relatively high and low by proper sizing of transistors. Figure 2(b) shows the first proposed level shifter, namely Contention Mitigated Level Shifter (CMLS).

In the CMLS, the above-mentioned contention is reduced, since MN1 and MP3 (MN2 and MP4) comprise a quasi-inverter. Therefore the logical values of node A and B are established faster than that of the conventional level shifter. Thus the delay of CMLS is less than that of the conventional level shifter. The power consumption of the CMLS is reduced compared with that of the conventional level shifter, because the contention reduction also brings in the crowbar current reduction.

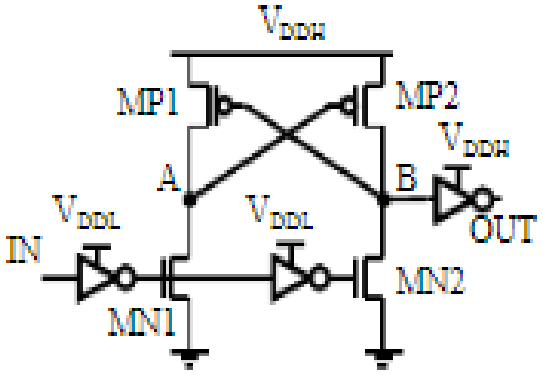
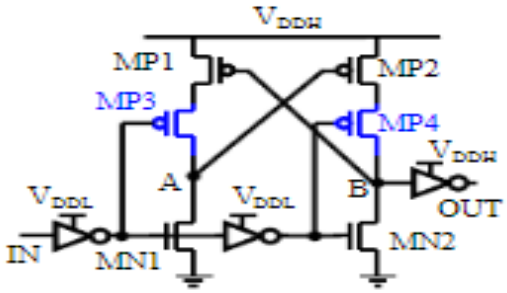


Figure 5. (a) Conventional level shifter.



(b) Contention mitigated level shifter (CMLS**).**

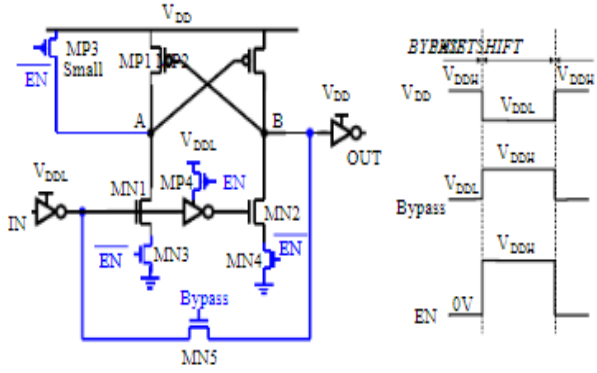


Figure 6 Bypassing enabled level shifter (BELS).

The waveforms of the signals Bypass and EN are also shown. In the block-level VDD-hopping scheme, VDD in one block is changed according to the performance needed for the block and it is known that for most of the

multimedia applications, the blocks are operated at VDDL for most of the time. Therefore, the speed and power at VDDL is very important. If the speed of shifter is faster in low-VDD environment, the VDDL can be reduced more aggressively, which in turn reduces power consumption further. Figure 3 shows the second proposed level shifter, namely a Bypassing Enabled Level Shifter (BELS). Two PMOS and three NMOS transistors are added to the conventional shifter. The BELS has two operation modes: "SHIFT" mode and "BYPASS" mode. When the output voltage VDD is high, that is, VDDH, the BELS is in a "SHIFT" mode. In the "SHIFT" mode, by setting the Bypass signal to VDDL, the contention at node B will be reduced and the logic value of node B is established faster. Therefore, the delay is less than the case of Bypass signal being set to 0V.

When the VDD is low voltage, VDDL, the shifting function is not required and the BELS is switched to "BYPASS" mode. In the "BYPASS" mode, signal EN is set to VDDH to cut off used transistors. Because the Bypass signal is set to VDDH in the "BYPASS" mode, MN5 can pass through signal without threshold voltage loss (Assuming that VDDH > VDDL + VTH).

3. DVS/DVFS/AVFS

Dynamic voltage and frequency scaling (DVFS) techniques—along with associated techniques such as dynamic voltage scaling (DVS) and adaptive voltage and frequency scaling (AVFS)—are very effective in reducing power, since lowering the voltage has a squared effect on active power consumption. DVFS techniques provide ways to reduce power consumption of chips on the fly by scaling down the voltage (and frequency) based on the targeted performance requirements of the application. Since DVFS optimizes both the frequency and the voltage, it is one of the only techniques that is highly effective on both dynamic and static power.

Dynamic voltage scaling is a subset of DVFS that dynamically scales down the voltage (only) based on the performance requirements.

Adaptive voltage and frequency scaling is an extension of DVFS. In DVFS, the voltage levels of the targeted power domains are scaled in fixed discrete voltage steps. Frequency-based voltage tables typically determine the voltage levels. It is an open-loop system with large margins built in, and therefore the power reduction is not optimal. On the other hand, AVFS deploys closed-loop voltage scaling and is compensated for variations in temperature, process, and IR drop using dedicated circuitry (typically analog in nature) that constantly monitors performance and provides active feedback. Although the control is more complex, the payoff in terms of power reduction is higher.

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IV. RESULT AND SIMULATION

Firstly, we have a tendency to use DSCH for logic design, Micro-wind for layout and power analysis DSCH for circuit design. DSCH is used to examine and verify the output responses of the logic circuit before the design will implement. DSCH jointly have the models, assembly support and symbols for the controllers like 8051 and 16F84. Designers can turn out logic circuits for interfacing with these controllers and verify package programs exploiting DSCH.

The Micro-wind package permits the user to articulate simulate an associated IC at the extent of physical description. Developed in city France, Micro-wind is associated innovative CMOS design tool for tutorial market. Micro-wind is developed as comprehensive package on windows platform to permit students to review smart and economical field of study methods and techniques with extra exercise. With constitutional layout sterilization tools, mix-signal machine, MOS characteristic viewer and etc. it permits students to review complete field of study technique with ease. Micro-wind unifies schematic introduction, pattern basically depended machine, Verilog extractor, netlist extraction, layout

compilation, cross sectional & 3D viewer, on layout mix-signal circuit simulation, BSIM4 tutorial on MOS devices, SPICE extraction of schematic and sign-off correlation to deliver unmatched style performance and productivity. By virtue of its sure approach for CMOS design education, Micro-wind has gained many followers worldwide. Universities across the worldwide are using Micro-wind for present students to show CMOS ideas with ease. Paving their path for a lot of expert package to be exploited at later stage of their course work.

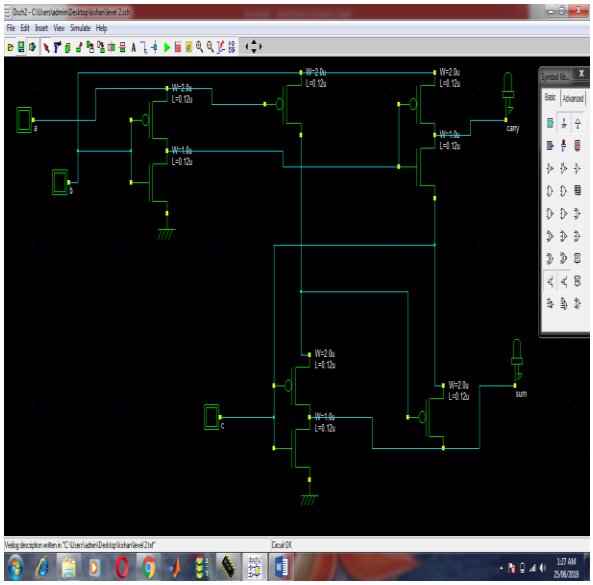

Figure 7 Level shifter circuit design dsch software.

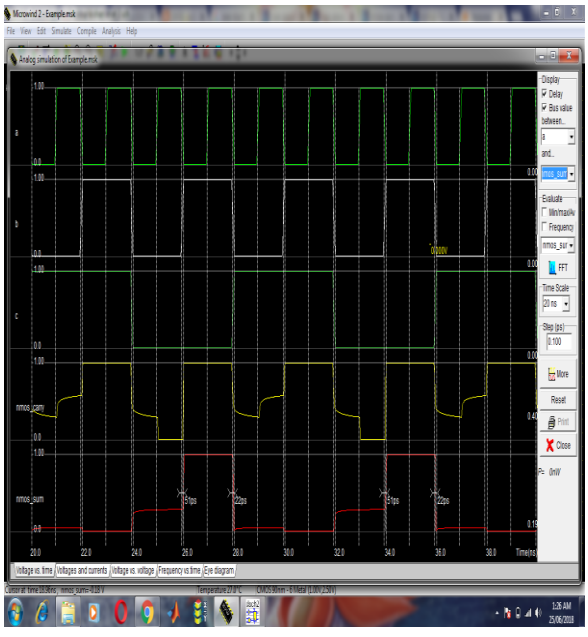

Figure 8 Level shifter circuit design MICROWIND software.

Design rules and electrical parameters

Layer	Width	Spacing	Surface	Surf capa	Lin capa	Ctk capa	Res	Unsalicid	Thickn	Height	Permitt
	lambda	lambda	lambda2	af/µm2	af/µm	af/µm	ohm	ohm	µm	µm	
nitride	0	0	0								
passiv	800	800	0								
metal6	8	8	100	30.00	35.00	45.00	0.03/sq	1.00/sq	1.60	6.20	2.40
via5	6	8	0				0.80/via		0.50	5.80	4.00
metal5	3	4	16	30.00	35.00	45.00	0.05/sq	1.00/sq	0.80	5.00	2.40
via4	2	4	0				0.80/via		0.50	3.95	4.00
metal4	3	4	16	25.00	25.00	40.00	0.15/sq	1.00/sq	0.35	3.60	2.40
via3	2	4	0				2.00/via		0.50	3.15	4.00
metal3	3	4	16	25.00	25.00	40.00	0.15/sq	1.00/sq	0.35	2.80	2.40
via2	2	4	0				2.00/via		0.50	2.35	4.00
metal2	3	4	16	25.00	25.00	40.00	0.15/sq	1.00/sq	0.35	2.00	2.40
via	2	4	0				1.00/via		0.50	1.55	4.00
metal	3	4	16	28.00	42.00	35.00	0.15/sq	1.00/sq	0.35	1.20	2.40
poly	2	3	16	80.00			4.00/sq	40.00/sq	0.20	0.01	4.00
poly2	2	2	8				4.00/sq	40.00/sq	0.20	0.27	4.00
contact	2	4	0				2.00/via		1.20	0.00	4.00
diffn	4	4	16	350.00	100.00		25.00/sq	250.00/sq	0.40	0.00	4.00
diffp	4	4	16	300.00	100.00		30.00/sq	300.00/sq	0.40	0.00	4.00

Figure 9 Design parameters.

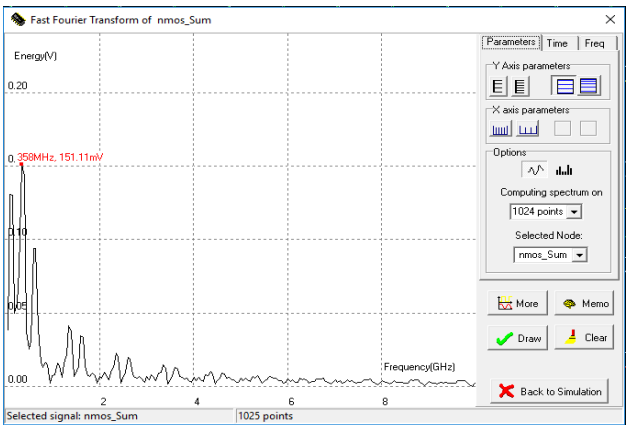

Figure 10 Shows the Fast Fourier Transform of nmos_sum.

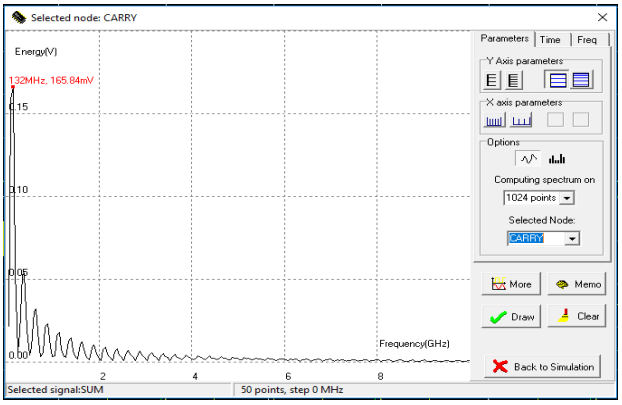

Figure 11 Shows the Fast Fourier Transform.

In the figure 5.5 we show that the layout designs of proposed Design which was generated in micro-wind layout tool. Shows that the results waveform voltage Vs time of proposed Design in micro-wind. Figure 4.13 and

4.14 depicted the results waveform voltage vs. current Design and results waveform frequency vs. time of proposed 14T Full Adder Design. Shows that the fast Fourier transform of NMOS sum and PMOS carry.

Table 1 Power consumption calculation:

Parameters	Base Paper	Our Proposed Method (DVFS)
Power Dissipation	5µW-15 µW	0.954 µW
Propagation Delay	12.2ps	0.1 ps

V.CONCLUSIONS

In this work, two basic level shifter circuit. Differential cascade voltage switch based level shifters and simple-inverter based level shifters are optimized for low power and high speed by using a novel device carbonado tube FET at 32-nm node. By setting the required chirality, minimum PDP is obtained by varying the number of nanotubes and applying back gate bias. Problems such as contention current (due to current imbalance) in DCVS-LS and the static leakage in both DCVS-LS and SI-LS are addressed carefully by proper selection of chirality and threshold voltage.

In present paper three new circuits of level shifters namely modified conventional, modified single supply and modified contention mitigated have been presented. Modified conventional level shifter gives power consumption of 5µW-15 µW for conventional level shifter. Proposed single supply shows power consumption of 0nw for conventional single supply. Third proposed circuit's shows power consumption of 396.75pW as compared to 0.4937354nW for existing circuit. Maximum output delay results also have been obtained for proposed circuits and it has been observed that with little concession in delay, power consumption has reduced considerably
A new level converter based on dualVth and feedback technique is proposed and compared to the best available level converter. The level converter is optimized for minimum power consumption and delay in 32 nm CMOS technology, the proposed level converter (DVF4) offers power savings up to 53% and delay savings up to 50%. DVF4 offers significant savings of 61% over benchmark circuits. A single-Vth.

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