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Silicon on Insulator Technology Review

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***Abstract*- An effort to reduce the power consumption of the circuit, the supply voltage can be reduced leading to reduction of dynamic and static power consumption. This paper introduces one of the greatest future technologies of this decade and that is SOI technology. Silicon-On-Insulator transistors are fabricated in a small (~100 nm) layer of silicon, located on top of a silicon dioxide layer, called buried oxide. This oxide layer provides full dielectric isolation of the transistor and thus most of the parasitic effects present in bulk silicon transistors are eliminated. The structure of the SOI transistor is depicted and is very similar to that of the bulk transistor. The main difference is the presence of the buried oxide it provides attractive properties to the SOI transistor. Power has become one of the most important paradigms of design convergence for multi gigahertz communication such as optical data links wireless products and microprocessor ASIC/SOC designs. POWER consumption has become a bottleneck in microprocessor design. For more than three decades, scientists have been searching for a way to enhance existing silicon technology to speed up the computer performance. This new success in harnessing SOI technology will result in faster computer chips that also require less power a key requirement for extending the battery life of small, hand-held devices that will be pervasive in the future. SOI is a major breakthrough because it advances chip manufacturing one to two years ahead of conventional bulk silicon. The following provides a step-by-step look at the developments leading up to the development of SOI technology.**

***Keywors*- SOI, ASIC/SOC, CMOS, VLSI, SIMOXT**

I. INTRODUCTION

In the 1960's the requirement for radiation hard devices in the military and space industry resulted in the development of silicon on-insulator devices. Due to the immature manufacturing processes, the manufacturers have been forced to use expensive materials to be able to create the active silicon on top of the insulating layer. Later processes have showed promising properties for the commercial sub nanometre technologies.

[1,4] this is why several of the recent CMOS processes are SOI processes and they are expected to become increasingly more common in the future. However, to design a system-on-chip using SOI, one has to be able to compensate for the unwanted effects on the analog circuits, which are due to the use of SOI Traditionally; the two most important criteria used for measuring the performance of a circuit have been speed and area. However, due to both increased transistor density and the advent of portable electronics an increasingly important cost measure in VLSI design is power consumption. [4,3] While recently a great deal of effort has been put into low power techniques for computation-intensive applications and SOI technology is one of them. Most of the early SOI devices were fabricated with SOS (Silicon-OnSapphire) wafers. The unique feature of today's SOI wafers is that they have a buried silicon oxide (Buried Oxide, or Box) layer extending across the entire wafer, just below a surface layer of devicequality single-crystal silicon. The active elements (e.g., transistors in a CMOS IC) of semiconductor devices are fabricated in the single-crystal silicon surface layer over the BOX. [2,1] The BOX layer provides robust vertical isolation from the substrate. Standard LOCOS (Local Oxidation of Silicon) or STI (Shallow Trench Isolation) processes are employed to provide lateral isolation from adjacent devices. [13,12,8] Most of the early SOI devices were fabricated with SOS (Silicon-On-Sapphire) wafers.

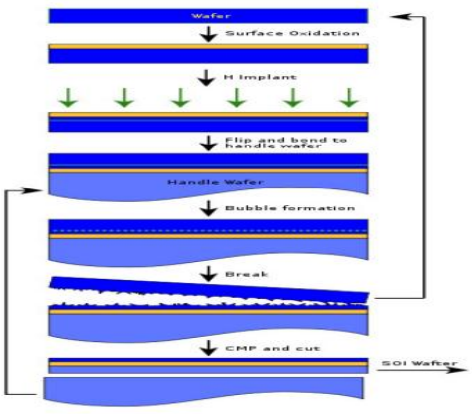

Fig.1. Fabrication of silicon on insulator through oxidation.

Alternately, SOI wafers can be fabricated by bonding a device quality silicon wafer to another silicon wafer (the "handle" wafer) that has an oxide layer on its surface. [45,44] the pair is then split apart, using a process that leaves a thin (relative to the thickness of the starting wafer), device-quality layer of single crystal silicon on top of the oxide layer (which has now become the BOX) on the handle wafer. This [27,1,2] is called the "layer transfer" technique, because it transfers a thin layer of device-quality silicon onto an oxide layer that was thermally grown on a handle wafer.

The "layer transfer" approach has led to the development of at least three production methods for fabrication of SOI wafers; SmartcutTM (UNIBOND) SOI wafers, NanocleaveTM SOI wafers, and ELTRANTM SOI wafers. The SmartcutTM and NanocleaveTM processes both employ high dose ion implantation (using hydrogen or other light species), either alone or in combination with other steps, to form a weakened silicon layer that splits (i.e., "peels off") the donor wafer, allowing the "layer transfer" to occur.

The ELTRANTM method (Epitaxial Layer Transfer) does not use ion implantation. It employs a layer of porous silicon, which is formed by anodic etching and annealing, to form the splitting layer. Recently, there is strong interest in SOI wafers for application to the fabrication of advanced CMOS ICs. [42] This is because SOI wafers provide a way to increase the speed performance of CMOS circuits, as well as reduce the power (and voltage) requirements to achieve high performance.

The trade-off between performance and power dissipation is the most fundamentally challenging issue on the horizon for scaling of CMOS ICs. [21,13] This issue threatens the roadmap of continuous scaling of CMOS devices. [14,10]A solution must be found to insure the commercial dominance of CMOS ICs in the future, so it is little wonder that SOI, which offers solutions to this issue, is receiving serious attention at leading-edge companies developing advanced CMOS ICs.[22,18,17] Compared to similar circuits fabricated on bulk silicon wafers, CMOS circuits fabricated on SOI wafers can run at 20-35% higher switching speeds than bulk CMOS, or 2 to 4 times lower power requirements when operating at the same speed as bulk CMOS.

II. SOI PROSPECTS

SOI wafers are now viewed as the most important emerging wafer engineering technology for use in leading edge CMOS IC production during the next 3-5 years [15]. One plausible scenario during this period is the rapid adoption of SOI wafers in place of epitaxial silicon wafers now employed as starting substrates for high-end logic device (e.g., microprocessors) and SOC (System on Chip) applications at the 0.13- and 0.10-micron technology nodes.[3] SOI wafers appear to offer an excellent platform for integrating RF and digital circuits on the same chip. Major semiconductor market research firms have forecasted the possibility that SOI wafers may make up 10% of all silicon wafers used by 2010.

Almost all of the "top 20" chipmakers have publicly expressed high interest in the inherent advantages of SOI wafers (e.g., IBM, Intel, AMD, etc.). A bright spotlight was cast on SOI wafer technology production in August 1998 due to an IBM announcement that they would adopt SOI wafer technology using the SIMOX SOI wafer process in high volume manufacturing on leading edge microprocessor architecture. It is in production now, using partially depleted transistor architecture [3,11]. Furthermore, Intel has recently unveiled their vision of the CMOS device they will pursue in the future, to achieve continuous scaling of CMOS with high performance and acceptable power (and voltage) requirements.

This is the Intel "Terahertz Transistor", which employs the use of a fully depleted (FD) CMOS transistor on thin SOI wafers [7], among other design changes (such as high-K gate dielectric and raised source-drain regions).

One of the more compelling reasons why support for migration from bulk to SOI CMOS is growing is due to the problems created by the exponential growth of the power dissipated by high performance, high density CMOS ICs in bulk (or epitaxial) silicon as scaling has been pursued [7]. For example, as Intel microprocessors have evolved by scaling through the 286, 386, and 486 generations into and through the Pentium generations, power dissipation has dramatically (exponentially) increased.

The 286 generation ran warm (to the touch by your fingers), the 386 ran very hot, and the 486 ran so hot that it needed a small fan to cool it. As evolution proceeded through the Pentium generations, the cooling requirement was more demanding at each generation, using more powerful fans and adding cooling fins to the microprocessor package to improve heat transfer out of the IC.

Assuming that the Intel microprocessor stays on its historical trend lines (Moore's Law), in 2005 ICs had about 1 billion transistors and operate at about 10 Gigahertz [14,9]. They will also dissipate so much power that they would require cooling by refrigeration of a liquid coolant in good thermal contact with the IC package. This is unacceptable as a computer systems requirement, and it illustrates that power dissipation is becoming a major barrier to scaling high performance, high density CMOS in the very near future. SOI CMOS offers a way to avoid this barrier without sacrificing high performance or high density.

SOI devices also appear to offer a sustainable, long-term pathway beyond the multiple barriers to scaling planar, bulk CMOS to 50n and below [1,38]. If the present understanding of the barriers and problems to scaling planar, bulk CMOS below 50nm is correct, then it is expected that a dramatic shift to fully depleted SOI CMOS will occur in the [11,7,7] 2006-2008 timeframe. If the many challenges in the fabrication of "ultra-thin" SOI wafers are met (adequate materials quality and acceptable cost), and if device design and lithography challenges are met, the way to 25nm CMOS is open, enabled in part by SOI substrates. SOI wafers will have a very significant impact on both the IC fabrication process and process equipment.

For example, [42,20] SOI wafers create a requirement for new types of ion implantation process equipment. [19,9,8] most SOI wafers are fabricated using an ion implantation step employing a high dose of oxygen (Ibis' SIMOXTM SOI wafer process) or hydrogen (SOITEC's SmartCutTM SOI wafer process).

III. SOI ADVANTAGES

The SOI [36] wafer structure has several important advantages over CZ bulk or epitaxial starting wafer architectures. SOI wafers potentially offer "perfect" transistor isolation (lower leakage), tighter transistor packing density (higher transistor count/higher IC function at the same lithographic resolution), reduced parasitic drain capacitance (faster circuit performance and lower power consumption), and simplified processing relative to bulk or epitaxial silicon wafers.

Due to these advantages, SOI wafers appear ideal for leading edge integrated circuits with high speed, high transistor count, low voltage/low power operation, and battery-operated systems requirements, such as portable logic or microprocessor ICs. Silicon-on-insulator (SOI) wafers have traditionally been used for extreme environmental applications, such as high temperature and severe environments (e.g., outer space). However, they are expected to expand into mainstream CMOS applications due to these advantages:

- Excellent lateral [40.20] and vertical isolation of active devices from substrate
- Elimination [5,6] of inter-device leakage and latch-up in CMOS structures
- Effective [11,5] reduction of substrate coupling in RF circuits (allows higher quality inductors with increased Q factor)
- Effective reduction [4,6] of interference and cross-talk between devices in mixed-signal ICs
- Different [6,12] voltages may be used on different devices without the added processing steps required for triple wells

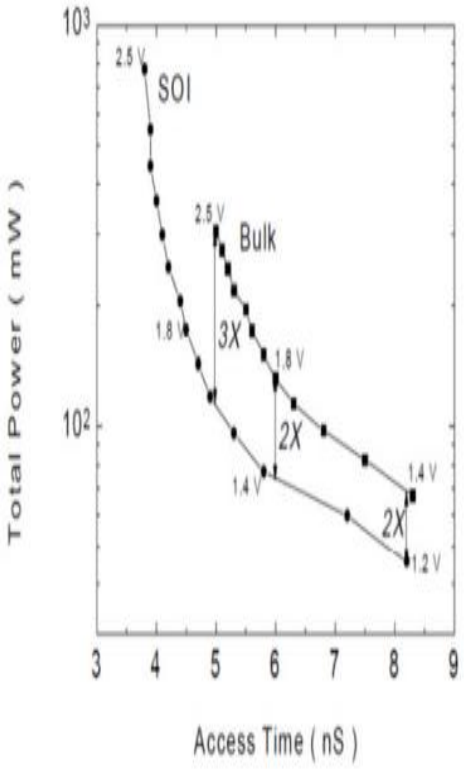

Fig.2.Improvement in execution time by using SOI

- Faster [37,41,1] device operation (speed/power product) due to reduction of parasitic capacitance (primarily due to reduced source-drain junction capacitance, but also from gate-tosubstrate capacitance and metal-to-substrate capacitance):
- IBM reported a [2,30] 20% to 35% increase in chip speed for their PowerPC chips.
- Lower power [23,31,12] consumption (speed/power product) due to lower operating voltages on devices and lower parasitic capacitance.
- IBM [13,11,2] reported a 35% to 70% reduction in power consumption for their PowerPC chips.
- More functions [43,32] per die area or reduced die area per function; SOI [10,9] allows tighter layout design rules (higher integration density), mainly due to reduced STI layout area required for lateral junction isolation (resulting from the absence of wells and the possibility of direct contact of the source-drain diodes in the NMOS and PMOS transistors)
- Performance [9,33,24] improvement equivalent to next technology node without scaling (e.g., performance of 0.25-micron devices on SOI wafers equivalent to performance of 0.18-micron devices on bulk wafers).

IV. COMPARISON BETWEEN SOI CMOS AND BULK CMOS

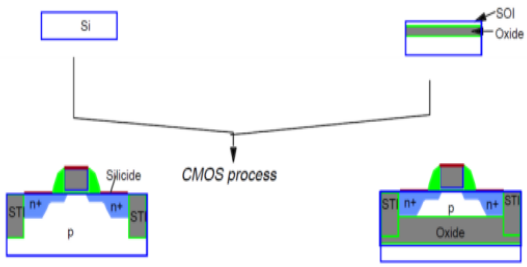

Fig.3. comparison between SOI and bulk CMOS

The difference between bulk CMOS and SOI CMOS are following:;

- [23,14,43] Today we are settling everything in small area. When scaling down the device dimensions the doping densities must be increased to maintain proper device behaviour, [44,8] which is hard to manage when the device dimensions reach 50 nm and below. However, for thin film devices, such as fully depleted SOI, the doping densities required are lower. This is one reason for why SOI may be more suitable for the future processes in comparison to bulk CMOS
- The [9,8,8] speed in bulk devices is much determined by the relative magnitude of the parasitic drain and source junction capacitances compared with the gate capacitance, which is increasing as the devices are scaled down and doping levels are increased.
- The [9,8,9] parasitic capacitances of the devices are thereby much smaller in SOI technologies than in bulk technologies. The active volume of silicon is smaller in SOI devices than in bulk technology. The SOI devices are therefore less sensitive to high energy particles and make them suitable for use in radiation hard applications.
- The increases of battery powered equipment strongly increase the demand for integrated circuits operating at a low supply voltage and with minimum power consumption [13,39,28]. This is also a reason for choosing SOI instead of bulk in the future, [20,42] since it is more suited to low voltage applications. In addition, the current drive capability of SOI devices is higher than for bulk devices, which increases the speed of the device. It [3,22] also makes it possible to trade speed/power, to get a device with the same speed performance as the bulk device, but at lower power consumption.

Future Soi Applications

After [3,1] criticizing SOI technology Intel Corp. is now adopting this technology again. Intel is now endorsing SOI with 22nm process technology. Intel will introduce a germanium (III V) channel and full depleted SOI at 22nm. In the recent several quarters Intel has revealing pieces of information about 22nm process technologies that will be used to manufacture Ivry Bridge-generation of microprocessors as well as system-on-chip devices. The Santa Clara, california based maker of central processing unit displayed its first 22nm test wafer with SRAM memory as well as logic circuits to be used in future Intel microprocessor. Intel has said that in case of 22nm fabrication process Intel's research group had a variety of novel transistors and interconnect ideas in pipepline including III-V channel materials, multigate transistors, 3-D stacking and others.

V. SOI CHALLENGES AND ISSUES

The [15,34,7] main barrier to the widespread adoption of SOI wafers for mainstream CMOS fabrication in the past has been the uncertain material quality and the higher cost of SOI wafers. However, these wafers are now demonstrating technical (materials quality) and economic (cost) readiness for use in mainstream CMOS IC production. [35,44,24] The key materials quality issues are the continuity and thickness uniformity of the BOX and the defectivity and thickness uniformity of the device-quality, single-crystal silicon layer.

Important BOX defects include voids and inclusions; [16,36,25] the defects in the silicon top layer include threading dislocations and pits (COPs). Also, the interface charge trapped at the interface of the top silicon layer and the BOX must be kept small (less than ~1011/cm2). [The amount of charge at the BOX/silicon layer interface affects the electrical behaviour of SOI CMOS transistors, e.g., threshold voltage and saturation current. [5,16,26]

The suppliers of SOI wafers continue to aggressively improve materials quality and reduce cost, driven by the considerable economic motivation of a rapidly growing commercial market for SOI wafers and a clearly defined roadmap for SOI material quality on the ITRS Roadmap [8,5,45,6]. In this fast-developing arena, reports of SOI materials quality measurements that are only a year old may be out of date.

Assuming [26,7,8] that the issues of materials quality and cost will be adequately addressed, the adoption of SOI wafers for CMOS fabrication is a non-trivial task. Fabricating CMOS devices in SOI presents challenges in device design and process integration, as well as in the process simulation, device simulation and circuit simulation TCAD tools. For [41,17,5] example, dopant diffusion in the thin silicon layer over the BOX is dramatically altered in SOI by interaction of the diffusing dopants with the silicon/BOX interface (at the top of the BOX) [14,46]. This and other differences must be comprehended in process simulations and in process integration for IC fabrication. Adopting SOI wafers is not a simple transfer of a bulk CMOS device fabrication

process into an SOI substrate. There [27,13,12] are also significant differences between the way a bulk or epitaxial silicon CMOS device and an SOI CMOS device behave electrically. For example, "short channel effects" (SCE) are typically suppressed more effectively in SOI CMOS devices than in bulk CMOS, and SOI CMOS devices typically have lower subthreshold leakage ("off current") and higher saturation current ("on current") than bulk CMOS counterparts [5,11,18,37].

Consequently, the SOI CMOS circuits typically demonstrate higher speed performance and lower power dissipation than bulk or epitaxial CMOS. Also, the SOI CMOS device exhibits several parasitic phenomena that are not typically observed in the bulk or epitaxial CMOS device [5,6,12].These phenomena are related to impact ionization in the high electric field that occurs near the drain in CMOS devices, and the fact that the channel terminal in the SOI CMOS device is isolated from the substrate, unless specific measures, such as body ties [6], are explicitly employed. In other words, the body of the SOI device is "floating".

There are several anomalous electrical behaviours in SOI CMOS devices that arise from these "floating body effects" (such as a "kink" in the output I-V characteristic of the SOI CMOS device and degraded drain breakdown voltage). Note that floating body effects are not necessarily all bad, as they may be employed to increase the current output from an SOI CMOS device [6]. The point is that the SOI CMOS transistor is different than the bulk CMOS transistor and these differences must be reflected in the simulators employed to design devices and circuits for CMOS Ics fabricated in SOI wafers. SOI CMOS transistors also exhibit so-called self-heating effects [5,6,13]. These effects arise in SOI devices because the device is thermally insulated from the substrate by the buried oxide (BOX). Consequently, removal of excess heat generated within the device-by-device switching is not removed as efficiently in SOI devices as it is in bulk devices.

This leads to a substantial elevation of temperature within the SOI device (50-1500C). This modifies the output I-V characteristics of SOI devices, once sufficient power has been dissipated within the devices. Note [3,4,6] that this self-heating effect only appears when power is being dissipated within the device (that is, when the transistor is on, conducting current through its channel). This [7,4] only occurs in CMOS circuits when a logic stage is switching state, not when it is in a stand-by state (e.g., holding a logic high or low state). These effects certainly will not [2,4,29] prevent the widespread adoption of SOI for CMOS ICs, but they must be taken into account by thoughtful device and circuit design approaches that specifically address the peculiarities of the SOI CMOS transistor vs.

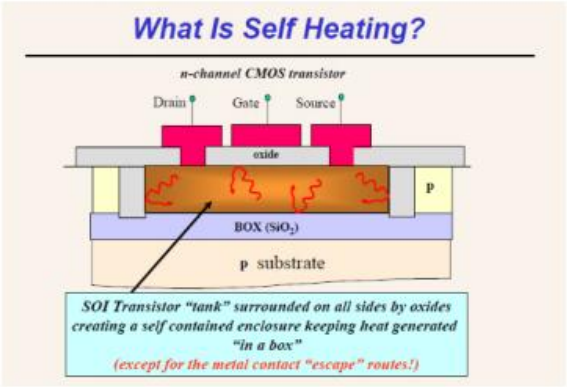

Fig.4. Self heating effect in SOI transistor.

the bulk or epitaxial wafer CMOS transistor. Obviously, the process [8,5,3] simulation, device simulation, circuit simulation, and layout TCAD tools employed by designers must accurately model the peculiarities and advantages of SOI CMOS to achieve optimal device design, circuit design, layout and processing approaches for CMOS ICs fabricated with SOI wafers. CMOS transistors designed for use with SOI wafers are classified by the thickness of the device-quality single-crystal silicon layer (at the surface above the BOX) relative to the depths of the source-drain junction and channel depletion layers in the device with the operating voltages applied. An SOI CMOS transistor is classified as "partially depleted" (PD) if the silicon surface layer is thicker than the depth of the depletion region in the transistor's channel.

The SOI CMOS transistor is classified as "fully depleted" (FD) if the silicon surface layer is equal to the depth of the depletion region in the transistor's channel. The transistor will be partially depleted or fully depleted depending on the silicon layer thickness above the BOX and the doping concentration in the channel. To form a fully depleted SOI transistor, the channel doping concentration must be low enough the gate depletion region extends throughout the entire thickness of the silicon layer. When the silicon surface layer is thicker than about 200nm, the transistor will typically be partially depleted, unless the channel doping concentration is reduced to such low values that the threshold voltage is too low for practical CMOS applications (less than 100mV).

If the silicon layer thickness is reduced to about 100nm, the transistor will be fully depleted, even when the channel doping concentration is increased to produce threshold voltages of 300-400mV. If the silicon layer thickness is reduced further (70nm), the transistor will remain fully depleted even if the channel doping concentration is increased to produce even higher threshold voltages (700mV). There are significant differences in partially depleted and fully depleted SOI CMOS transistors [5,34]. For example, the threshold voltage of the fully depleted

(FD) device is very sensitive to the silicon surface film thickness.

This results in an addition source of manufacturing variance in the fabrication of FD SOI CMOS. Typically, this is on the order of 10mV in threshold voltage per nanometer of variation in the silicon film over the BOX. This is the main reason why, at the present time, the fabrication of commercial CMOS on SOI typically employs partially depleted (PD) devices. However, careful device design and optimizing the channel implant process can reduce this sensitivity in FD devices.

It [5,8,6]is also important to note that the variation of drain (saturation) current does not have the same sensitivity to film thickness as the threshold voltage in FD SOI CMOS [5,16,35]. There are significant advantages for FD transistors over PD transistors, and the trend in SOI CMOS is toward the use of fully depleted devices. A fundamentally important point is that in FD SOI CMOS the subthreshold slope can be very low (less than ~65 mV/decade (i.e., a 65 mV increase in gate voltage will result in a tenfold increase in the subthreshold drain current).

This is [10,9] significantly closer to the theoretical minimum (~60 mV/decade) than the typical values of 80-85 mV/decade in PD SOI CMOS and 85-90 mV/decade (best case) in bulk CMOS. This is a critical advantage. It allows the threshold voltage of the FD SOI CMOS device to be very low (150-200mV) with acceptable subthreshold leakage ("off current"), which determines off-state power dissipation. Lowering [8,01] the threshold voltage also means that the supply voltage can be reduced significantly without degrading CMOS IC speed performance (the supply voltage needs to be 4-5 times the threshold voltage; below this ratio, the speed performance of the circuit will degrade rapidly).

The [47,7] reduction of the supply voltage produces a significant reduction in active (switching) power dissipation, without unacceptable performance degradation. [Note: [37,9] the active power dissipation is also reduced somewhat by reduction of parasitic capacitance in SOI CMOS relative to bulk CMOS.] Also, in the FD CMOS device the variation of threshold voltage with temperature is significantly less (2-3 times less) than in the PD CMOS device.

Furthermore, [38]in general, the anomalous electrical behaviours arising from floating body effects in SOI CMOS transistors are less of a problem in FD transistors than they are in PD transistors. Consequently, it is expected that FD SOI CMOS transistors will be generally adopted in the near future [1,8,48]. Converting an existing PD SOI CMOS device and circuit design into FD CMOS is expected to be straightforward [7,9], at least in comparison with to the challenges in the conversion from bulk CMOS to SOI CMOS.

VI. PERFORMANCE IMPROVEMENTS

Here some practical data is showing some comparison between SOI and bulk CMOS. We can see how much the performance is increased when we [49,6] are using the SOI CMOS-

- [41] SOI Ring oscillator frequency up to 20% higher
- [40] Inverter performance up to 10% better
- [39] 2 NAND up to 27% better
- 3 NAND up to 27% better
- 2 NOR up to 27% better
- 3 in NOR up to 25% better

VII.CONCLUSION

As the SOI technology becomes more of a mainstream technology it becomes increasingly important to be able to handle and compensate for the unwanted effects introduced when using SOI [48]. Some of the most important effects kink effect, history effect and self heating appears as the most important. Some methods to compensate for these effects were presented. In comparison with bulk the SOI technologies appear to be more suited for the future sub nanometer and low supply voltage technologies. The power consumption is also expected to decrease if SOI [6,7]is used instead of bulk devices.

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