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Performance Analysis of Single phase 7 level CHBMLI for Various Applications

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***Abstract*- Inverter is a device which is used for converting DC power into AC. Due to harmonic issue in conventional inverter researcher work in the field of multi-level inverter. A multi-level inverter starts from 3 level to n level. In the recent year due to increasing in renewable generation the scope of work in the field of multi-level increases day by day. The main work in this paper is to develop the easy topology for 7 level generations with the help of multilevel inverter. The proposed scheme is used for implementation for the different load which is used in domestic purpose. The multi carrier PWM technique is used for switching action. Finally the performance is verified by the use of MATLAB software by the experimental result. The THD is calculated for different load on proposed work.**

***Keywords*- digital DC to AC Converter, 2 Level, Renewable Energy, THD, and CHB 7 level MLI.**

I. INTRODUCTION

In real world most of renewable energy resources that has been used is a DC energy in nature such as solar energy ,wind, tidal and biomass, however the electrical transmission systems is in AC and not all of the loads (appliances/machines) are using the direct current (DC) power supply as their sources. Most of them need an AC power as their main source. This is where the inverter is needed to convert DC energy to AC energy.

Multilevel inverters have been under research and development for more than three decades and have found successful industrial applications. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years. Nabae[1] realized that with using more than 2 levels of voltage source converter, it would produce multiple ac voltages. Later on in 1981, the author proposed neutral point clamped MLI starting with three levels from which he introduced the idea of multilevel inverter. After that many authors discuss various topologies of multilevel inverter [2].

Since multilevel inverter inverters generate many voltage levels by translating dc voltage levels into multiple ac voltages, these are in great demand to use in the high power applications. Multilevel inverter uses dc source of voltages for incorporating voltage waveform with stair case approach and reduces harmonic contents. In 1975 R.H. Baker [3] introduced the concept of series inverter connection in the form of Hbridge. The aim was behind was that multiple voltages can be generated with the series connection of one phase inverter. Marchesoni M. et al. [4] had proposed the inverter topology known as cascaded H-bridge multilevel inverter. Since other topologies of MLI; Diode clamped and Flying capacitor inverter use clamping diodes and flying capacitor respectively make the circuit complex, to overcome these disadvantages, cascaded H-bridge inverter was proposed. From here, the basic idea was generated [1990] to connect single phase inverter in series with several separate dc sources. Following the above concept of series inverter connection, Further F.Z. Peng et al. [5] successfully realized the cascaded H-bridge multilevel inverter and labelled the disadvantages of DC-MLI and FC-MLI over cascaded inverters.

Many researcher [6-10] works in this field for developing the level of the multilevel inverter. Farid Khoucha et al. [11] first realized asymmetrical multilevel inverter. For this, symmetrical inverters were also realized for the comparison analysis purpose on the basis of switching components, dc sources, and switch losses. Using five and seven level, a comparison was done. Symmetric and asymmetric multilevel inverter topology is reviewed in [12-15].

Binary based asymmetric inverter is discussed in [16]. In paper [17], the author discusses the comparative investigation between various levels of asymmetrical topology on the basis of losses in the switches, harmonic contents. These inverters operated at low frequency. Giuseppe Carrara et al. [18] described a short conclusive test on a sub-harmonic PWM strategy for multilevel inverters for the triggering of switching pulses. For switching of multilevel inverter the multicarrier PWM strategy is discussed in [19-22]. This is the easiest method for switching of MLI. In this paper discuss the basic problem in conventional inverter and proposed single phase 7 level cascaded multilevel inverter. Next section

discusses the overall methods for making proposed model.

II. MULTI-LEVEL INVERTER

In the past decades, most of researches have focused in finding renewable energy resources which is environmentally friendly and reduce the full dependency on the fossil fuel resources which is the main factor for global warming and environmental pollution. Since most of the renewable energy resources produces a DC power in nature the invention of inverter has offered a greet solution to use these DC power as an AC power which the most frequently used by appliance and machinery. In the early decades the inverter used was the conventional two level inverter since the requirement was not as much as essential where the inverter was used to supply small load.

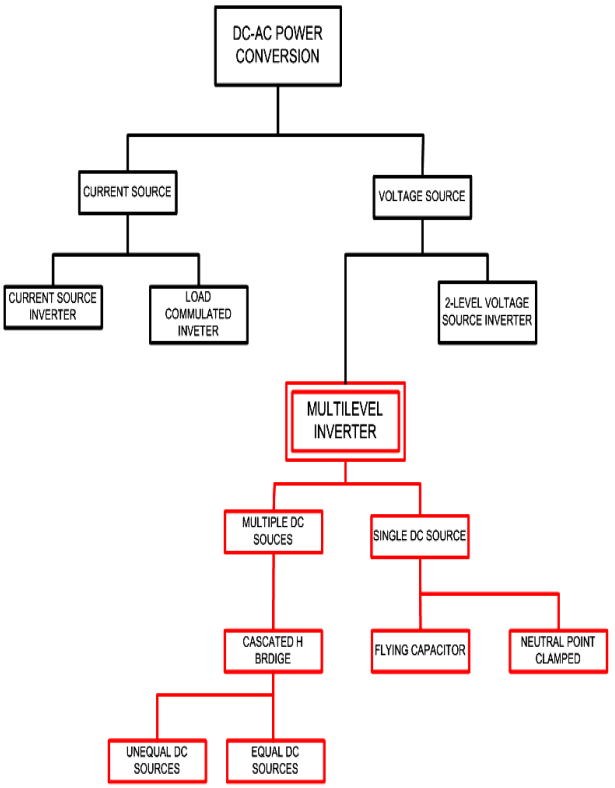

Fig.1. Classification of multilevel inverter.

However the inverter has attracted a large interest to be used in heavy duty industries and high power application but with the rapid growth in the industry and introducing the higher power application equipment which reaches the megawatt level it is hard to connect a single power semiconductor switch (conventional two level inverter) directly to medium voltage grids, also the two level inverter with higher harmonic distortion which need a complex filtering circuit to get the sinusoidal waveform. Due to this drawbacks of the conventional two level inverter, it recommended to use the multilevel inverter (MLI) which has many advantages compared to single stage inverter like minimum harmonic distortion which produce almost sinusoidal waveform without filtering circuit, also the MLI can operate with high power applications and produce high level output voltage with less switching losses and reduced contents. Thus the MLI is recommended not only for the use in high power applications but it can be used for industrial applications as alternative in high power and medium voltage situations. Fig 1 shows the classification of the multilevel inverter.

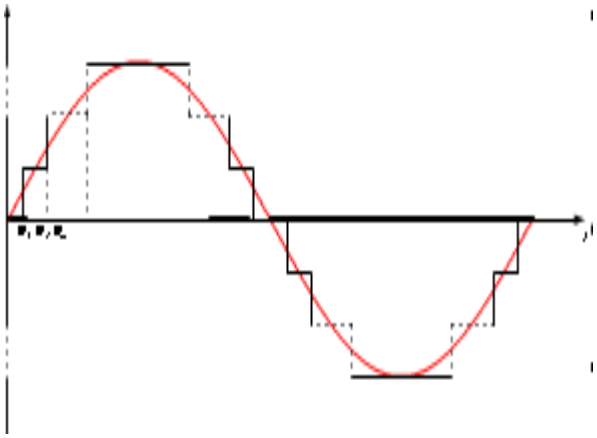

Fig 2. Generalized Stepped Waveform of MLI.

Multilevel inverter utilize an arrangement of power semiconductor switches and a number of lower voltage DC sources to approach with a stairs output voltage wave shape as with variable and manageable frequency, section and amplitude. Multiple DC voltage sources like batteries, capacitors and renewable energy resources are used in Fig. 2. Shows the generalized stepped waveform of the MLI. In the generalized wave shape, Ɵ1, Ɵ2……..Ɵn are the change in switching angles. Each the widths and heights of the steps are often adjusted. However, heights of the steps are typically created equal and solely widths are adjusted per the specified wave shape by changing the switching angles.

III. CASCADE H-BRIDGE INVERTER

The However, there are different topologies of multilevel inverter and each topology perform in its own fashion and has different methods of producing switching sequences, but there are some challenges that MLI faces offered by its topologies. Like, diode clamped and flying capacitor multilevel inverter, cascaded H-bridge MLI does not use separate dc sources. The concept of using separate dc sources in individual bridges is that achievement of various voltage levels without occurrence of short circuit which can take place with same dc sources. DC-MLI needs so many clamping diodes which make generally the circuit complex. Also FC-MLI uses capacitors which are known for balancing, cause voltage sag problems. To overcome the limitations of both topologies cascaded H-bridge (CHB) multilevel inverter had been proposed.

By cascaded H-bridge MLI, we mean one or more elements of H-bridge are connected in a series link to produce the desired ac output voltages. These bridges are look – alike of an alphabet "H". H-bridge represents electronic circuit in which voltage is applicable across the load. CHB MLI uses separate dc sources and does not require clamping diodes and capacitors as needed by DC-MLI and FC-MLI respectively. This topology is quite cheaper than the other two. It promises low harmonic content and has excellent features in high power and high voltage applications. CHB-MLI has overcome the disadvantages of DC-MLI and FC-MLI in the sense that number of switching components required in cascaded H-bridge inverter is less compared to the others. So, it reduces the cost. The series connection allows it to achieve high as well as medium voltages and power also. Separate dc voltage sources and H-bridge are the basic blocks for CHB- MLI. The output voltage with respect to the ground is given by the equation.

$$V_{on} = \sum_{i=1}^{N} V_i$$

Where N is the number of H-bridge cells. The above equation is showing the final voltage is equal to the addition of voltage of each H-bridge cell.

The cascaded H-bridge inverter has drawn tremendous interest due to the greater demand of medium-voltage high- power inverters. It is composed of multiple units of single- phase H-bridge power cells. The H-bridge cells are normally connected in cascade on their ac side to achieve medium voltage operation and low harmonic distortion. The cascaded H-bridge multilevel inverter requires a number of isolated dc supplies, each of which feeds an H-bridge power cell.

IV. PROPOSED 7 LEVEL CHBMLI

To synthesize a multilevel waveform, the AC outputs of each of the different level H-bridge cells are connected in series. The cascaded voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by:

$$N = 2s + 1$$

Where, s is the number of DC source. The number of switches requirement is given by:

$$Nswitch = 4s$$

Voltage on each Stage can be calculated by using equation.

$$Vs = s\ Vdc$$

For generation of 7 level it require 3 DC voltage source from the above equation [2]. The multilevel inverter consists of full bridge modules with output waveform of seven level

$\pm 3V_{dc,} \pm 2V_{dc,} \pm V_{dc,}$ *and* 0

Fig. 3 shows the proposed 7 level CHBMLI.

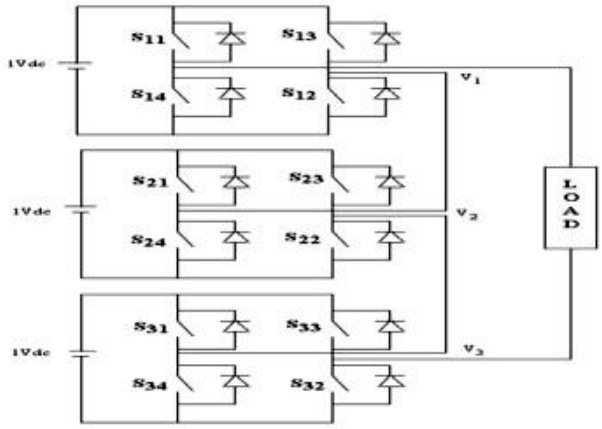

Fig 3: Schematic Diagram of Proposed 7 Level CHBMLI.

The relationship between the switching states and output voltages for Fig 3 is shown in Table 1. In Table 1, the sign '+' and '-' indicate the output voltages of the upper stage and lower stage respectively. Zero ('0') indicates that the associated stage is in freewheeling state, which means that output terminals are connected to the positive (or negative) DC link. The phase voltage is the sum of each H-bridge outputs and is given by

Table 1. Switching of Separate DC voltage for Proposed 7 Level CHBMLI.

O/p Voltage	SM1	SM2	SM3
$3V_{dc}$	+1	+1	+1
$2V_{dc}$	0	+1	+1
	+1	+1	0
	+1	0	+1
V_{dc}	+1	+1	-1
	+1	-1	+1
	-1	+1	+1
	0	0	+1
	0	+1	0
	+1	0	0
0	0	0	0
	+1	-1	0
	-1	+1	0
	+1	0	-1
	-1	0	+1
	0	+1	-1
	0	-1	+1
$-V_{dc}$	-1	0	0
	0	-1	0
	0	0	-1
	+1	-1	-1
	-1	+1	-1
	-1	-1	+1
$-2V_{dc}$	0	-1	-1
	-1	0	-1

	-1	-1	0
$-3V_{dc}$	-1	-1	-1

V. MULTI CARRIER PWM

In this section, the devised control technique is explained. It is developed in a manner that it will be applied to all or any topologies of converters A schematic drawing of the proposed scheme is shown in Fig.4.

For a presented converter, let the number of levels in the phase voltage be nlevels. A voltage source inverter allows multilevel operation if nlevels ≥ 3. Since level 0 is obviously important, nlevels is considered to be odd. Also, number of positive levels in an nlevels waveform will be:

$$n = \frac{(n_{levels} - 1)}{2}$$

The modulating (or reference) signal, fref (t), is a waveform with amplitude Aref and angular frequency ωref. There should be 2n carrier signals for nlevels number of output levels. These carriers have the angular frequency car and peak-to-peak amplitude Acar. Carrier signals above the zero reference are chosen as f +car, j (t) and those below the zero reference are designated as f – car, j(t) , { j = 1 to n }. Carrier signals are displaced such that they engage immediate bands and zero reference is positioned in the middle.

Stage Comparator

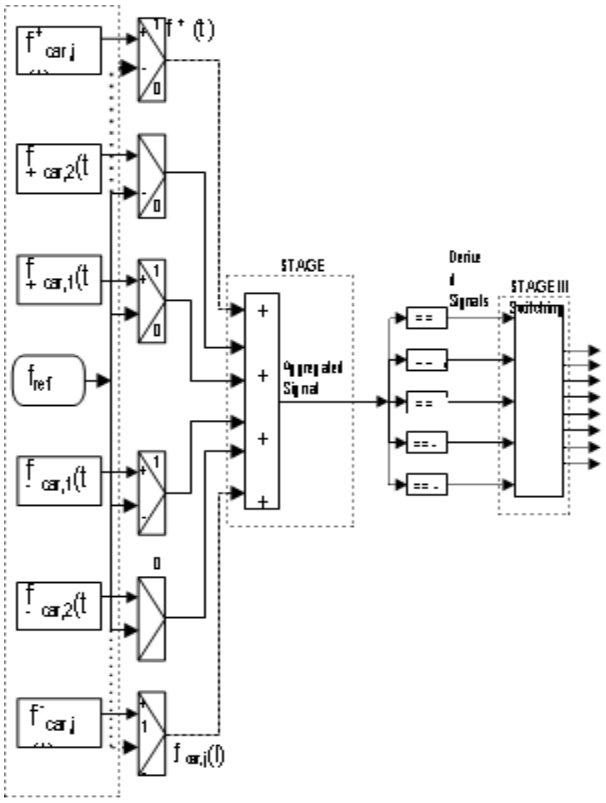

Fig 4. Control Strategy for the proposed & level CHBMLI.

At each instant, each carrier is evaluated with the modulating signal. For all the carrier signals on top of the zero reference, every comparison gives '1' if the modulating signal is greater than the carrier and '0' otherwise. For all the carrier signals below the zero reference, each comparison confers '0' if the modulating signal is superior than the carrier and '-1' otherwise. That is,

f + out, j(t) =1, for fref (t) ≥ f + car,j(t) = 0, otherwise
f - out, j(t) = 0, for fref(t) ≥ f ¬ car,j(t) = -1, otherwise

VI. RESULT & DISCUSSION

For validation of proposed work as discussed in previous section Fig 5 shows the MATLAB/SIMULINK model. Table 2 shows the parameter used in the simulation process. For generation of 7 level here use 3 separate dc sources and 12 switches, 4 in each H-Bridge cascaded inverter. Table 2 shows the parameter used in the simulation. Fig 5 to 12 shows the current and voltage generated due to R and R-L load. The FFT analysis of each waveforms gives the THD of the system.

Table 2. Parameter used in the simulation

Parameter	Value
DC Source input for each H-Bridge	100 V
Number of DC source	3
Number of Switch (MOSFET)	12
Output voltage (AC)	300 V
Level of output	7
Carrier Wave frequency	1 kHz
Load Resistance	20Ω
Load Inductance	50 mH

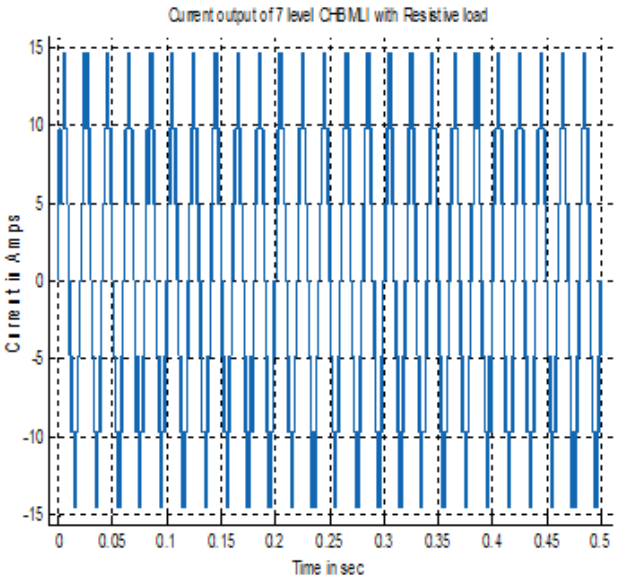

Fig 5. Current Response of proposed Work with resistive load

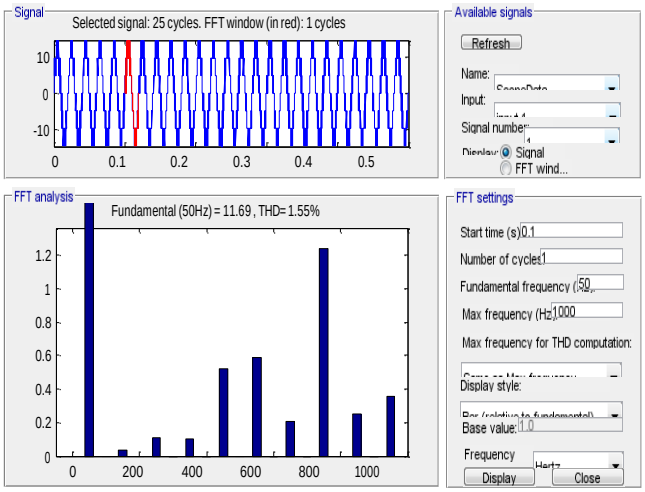

Fig 6. FFT Analysis of current of proposed work with Resistive load.

Figure 5 shows the output current of purely resistive load with FFT analysis. The result is stepped output with lower THD. Figure 6 shows the THD generated in the proposed work. The total harmonics distortion is given by 1.55% at fundamental current 11.66 A

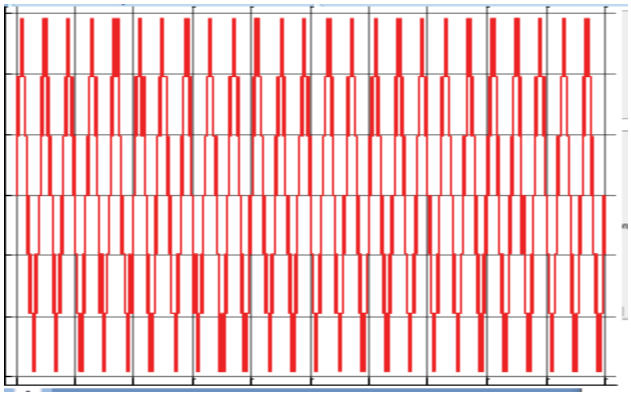

Fig. 7. Voltage response of proposed work with R load.

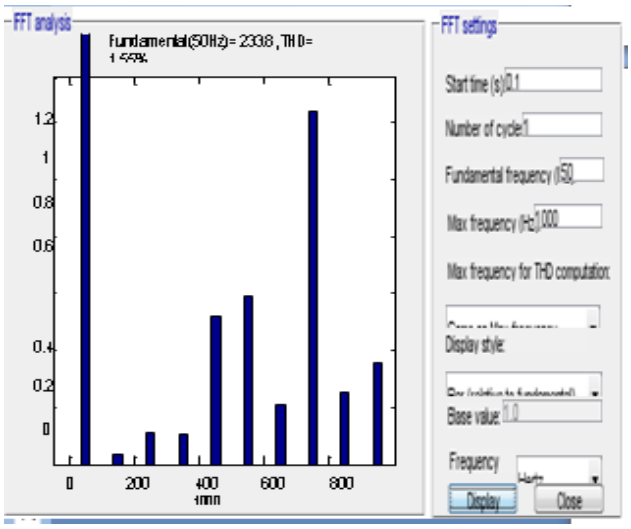

Fig 8. FFT analysis of voltage of resistive load.

Fig 7 and 8 shows the output voltage of purely resistive load and their FFT analysis. The result is stepped output with lower THD. THD generated in the proposed work. The total harmonics distortion is given by 1.55% at fundamental voltage 233.8 V.

Fig 9 shows the output current of R-L load. The result is sinusoidal due to nature of inductor. Figure 10 shows the THD generated due to current of R-L load in the proposed work. The total harmonics distortion is given by 0.22 % at fundamental current 9.28 A.

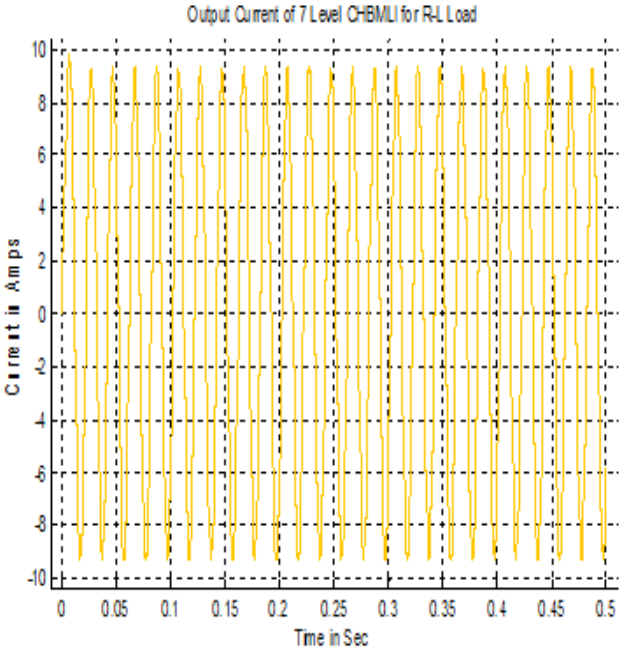

Fig.9. Current Behavior of R-L Load in proposed CHBMLI.

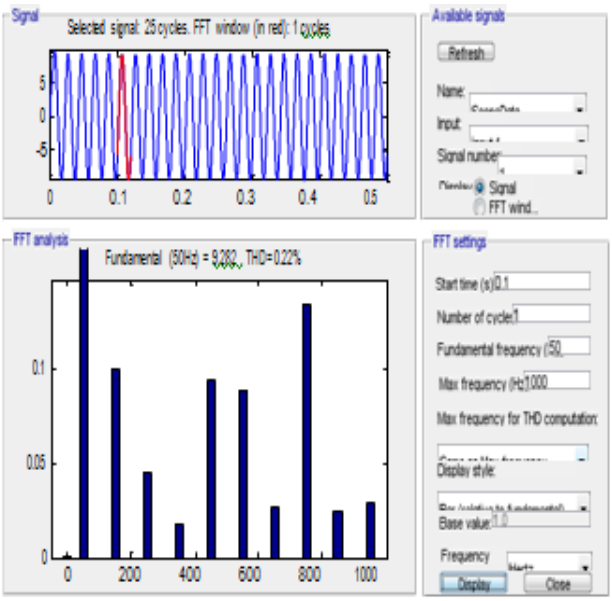

Fig 10. FFT analysis of current of R-L Load

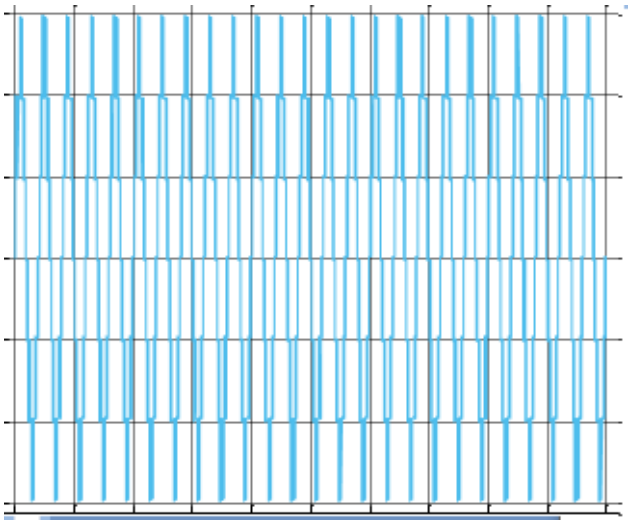

Fig 11. Voltage response of proposed work with R-L Load.

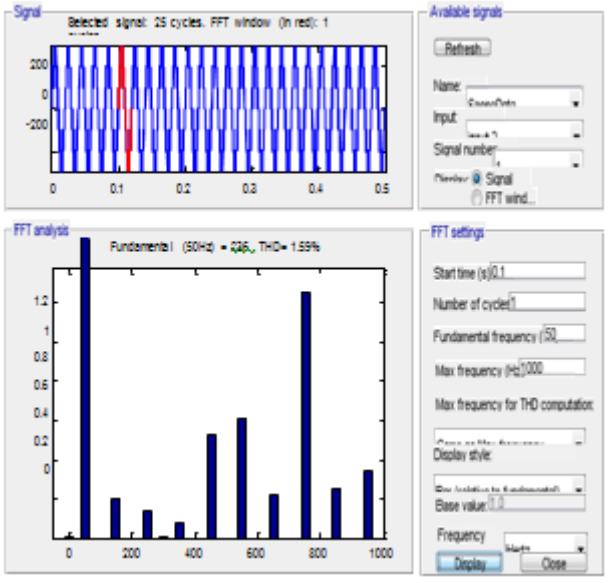

Fig 12. FFT analysis of voltage of R-L load.

Figure 11 shows the output voltage of R-L load. Figure 12 shows the THD generated due to R-L load in the proposed work. The total harmonics distortion is given by 1.59% at fundamental voltage 236 V.

VII. CONCLUSION

Cascade Multilevel is the example of generation of the high level output with the help of single H-Bridge inverter in series. In this paper developed single phase low voltage 7 level cascaded H-Bridge Multilevel inverter. So formation of the CHBMLI separate DC source technology is used. The multicarrier PWM technique is used for pulse generation for the proposed CHBMLI. The whole work is simulated in MATLAB/SIMULINK environment. The result is verified for different type of load. The THD varies between 0.22 to 1.92% in the current and voltage of the output in the proposed CHBMLI.

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