International Journal of Scientific Research & Engineering Trends
Volume 6, Issue 5, Sept-Oct-2020, ISSN (Online): 2395-566X

Design and Analysis of Low Power Consumption I0T Full Adder Circuit

M.Tech.Scholar Sheetal Sahani, Dr. Bharti Chourasia
Department of EC ,RKDF University,Bhopal,MP,India

***Abstract*-This paper presents a design methodology using CMOS transistor for the architecture of full adder design with minimum number of transistor i.e. reduced size and reduced area for low power consumption in CMOS 90nm technology. This is used to implement low power full adder design for carrying out summation of three different input bits. The circuit of low power full adder is designed by using DSCH tool 2.7 & analysis of the low power full adder design is done at room temperature in CMOS 90 nm technology by using Micro wind tool 2.6.The result shows the comparison in CMOS technology at 90 nm rule on the design in regards of power dissipation, signal propagation delay, transistor counts and power delay product. A comparison is also carried out by some of the parameters taking into consideration like delay of the low power full adder circuit design with the base paper full adder design, which shows the advantage of the proposed low power full adder design. We are using two different simulation tools such as DSCH 2.7 for circuit design and Micro-wind 2.6 for waveform simulation. Firstly the low power full adder circuit will be designed using DSCH tool 2.7 using 10 transistor maintaining W/L ratio 3:1. Then the Verilog code of the design is made and the layout will be made in CMOS 90 nm technology using microwind tool 2.6. The low power full adder circuit using 10T design will be simulated at room temperature in CMOS 90 nm technology to compare different parameters like power consumption, delay, PDP & transistor counts.**

***Keywords*-Full Adder, CMOS, DSCH, MICROWIND, Transmission Gate Logic**

I.INTRODUCTION

Full Adder is the heart of any central processing unit that is a core component employed in all the processors. Low-power design of VLSI circuits has been identified & has resulted in explosive growth of integration of sophisticated multimedia-based applications into wireless & mobile electronics gadgetry in the recent years. Full Adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation, etc. Energy conversion is needed to represent a change in signal value.

If energy exists only in one form, i.e. electric energy, then there is only one irreversible energy conversion from electric energy to heat. To break this one-way conversion, researchers have introduced another energy form, i.e. magnetic field energy, into the digital circuit. If one relates the signal change to the conversion of electric energy to magnetic energy the so-called "energy-recovery" can be realized. This is the method by which the irreversible conversion from electric energy to heat caused by dissipative elements, i.e. resistors, is largely reduced or avoided. The energy conversion from electric field to magnetic field and vice versa implies that circuits should be supplied with AC power. In this case, signals in the circuits should also be alternating quantities. The latter has been extensively used in dynamic CMOS logic, clocked CMOS logic and various domino logics. However, those circuits still rely on DC power, and the energy conversion remains as electric energy to heat. There is need for further study in the case of circuits supplied with AC power. The AC power controls the working rhythm of the circuit and acts as the clock, called the powerclock. Rest of the paper organize as follows: In the section 2 explain the related work results of various full adder design using different mechanism, problem statement describe in section 3, section 4 describe the proposed design and their mechanism and used simulation tool also, section 5 describe the simulation results of proposed hybrid design, last but not the least discuss the conclusion.

II. RELATED WORK

Madhu et al [1]: In this paper an energy-efficient hybrid 1-bit full adder design is reported. The main aim of our work is to achieve low power and high speed design goals. The proposed hybrid adder is used the combination of CMOS logic (Complementary Metal Oxide Semiconductor) and transmission gate (TG) logic. The circuit has been implemented using Tanner EDA tools in 90 nm technology. Performance parameters such as power and delay have been compared with the existing designs such as complementary pass-transistor logic based adder, transmission gate logic based adder, transmission function adder, hybrid adders, and so on. Power consumption of the proposed adder is found to be 0.1292 μw at 90 nm for 1.2 V supply and delay in the signal propagation is

measured as 0.0247 ns for 90 nm technologies. It means that proposed adder consuming extremely low power and low propagation delay than existing designs for the same testing environment.

M Nikhil Theja et al [2]: In this paper, hybrid logic style is adopted to design the full adder. The main objective of this design is to achieve Low power and high speed. Hybrid logic style used is the combination of C-CMOS logic (Complementary Metal Oxide Semiconductor) and Transmission gate (TG) logic. The Circuit was implemented using Micro-wind tool in 90nm and 180nm technology. Performance metrics of power and speed are compared with existing adder designs such as conventional CMOS adder, Transmission gate adder (TGA) and Transmission Function adder (TFA). Average Power consumption of the proposed design is found to be 1.114 µW at 90nm for 1.2V supply and 5.641 µW at 180nm for 1.8Vsupply. Delay in the signal propagation is measured as 0.011ns and 0.087ns for 90nm and 180nm technologies respectively.

Majid AminiValashani et al [3]: The research introduce that the full adder cells play a vital role in numerous VLSI circuits. Therefore, design of an energy-efficient full adder which operates reliably in submicron technologies has become a great concern in recent years. Some previously designed cells suffer from non-full swing outputs, high-power consumption and low speed issues. In this paper, two high-speed, low-power and full swing full adder circuits are designed in 90-nm CMOS technology. According to simulation results, the proposed circuits have rail to rail output signals. Also, an improvement of 12%-52%, 7%-48% and 28%-68% has been achieved in delay, power consumption and power-delay product (PDP), respectively.

S. Srikanth et al [4]: The research article proposed that the designing multipliers that are of high-speed, low power, and regular in layout are of substantial research interest. Speed of the multiplier can be increased by reducing the generated partial products. Many attempts have been made to reduce the number of partial products generated in a multiplication process one of them is array multiplier. Array multiplier half adder has been used to sum the carry products in reduced time. Achieving high speed integrated circuits with low power consumption is a major concern for the VLSI circuit designers.

III. PROBLEM STATEMENT

Performance factors such as power, delay, and layout area were evaluated with the existing designs such as C-MOS, Mirror, TFA, TGA,14T,HPSC,Majority Based,24T, FA _Hybrid ,FA_DPL , FA_SR_CPL, HYBRID FA & Hybrid logic. Due to toughness beside CMOS scaling and transistor sizing with the overhead of high input capacitance and requirement of buffers, the adder using this static CMOS. Also this design proves the power dissipation cause due to the stray capacitances and large length interconnects. The circuits design using CMOS logic with large number of transistors and maximum length interconnect are gradually more existing provider to propagation delay, overall area and power consumption. The main goal of this work is to improve the different function parameters such as power dissipation, path propagation delay and number of transistor used in full adder design compared with the previously existing ones. Floating point (F.P.) addition is a preferable operation for a wide range of applications. The main areas in which we work are area-efficient, dynamically configurable, multi precision architecture for F.P. addition. In our work the use of transmission gate decreases the number of transistors which overcomes the area tradeoffs. The main drawback of the parallel adder is that the delay rises linearly with the bit length.

III. PRPOSED MODULE DESIGN

An energy efficient low power consumption full adder unit has designed with DSCH tool using 10 transistors. The layout of low power consumption energy efficient full adder has create on micro-wind tool at two different nm technology 90 nm, and 180 nm and simulate with using Verilog language which has generated by the DSCH tool.

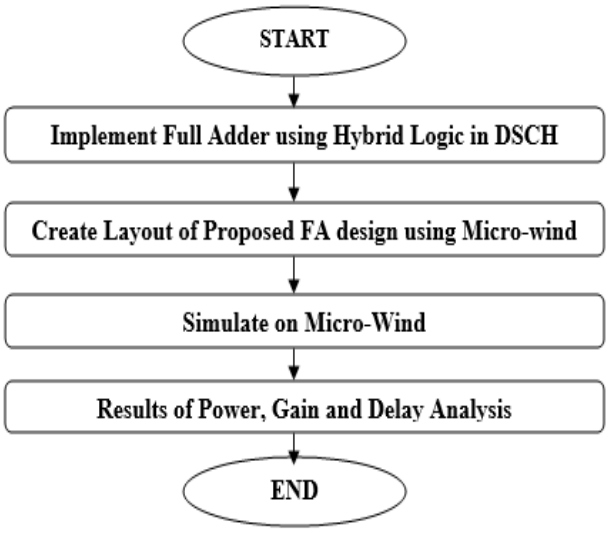

Figure 1 Essential Block and Step of Process.

In this proposed work, an energy efficient or low power consumption full adder unit with designed the hybrid logic i.e. combination of complementary metal oxide semiconductor and pass transmission gate logic. Full adder unit performed operation like addition. The layout has made on micro-wind tool for fabrication and power and waveform analysis of design methodology.

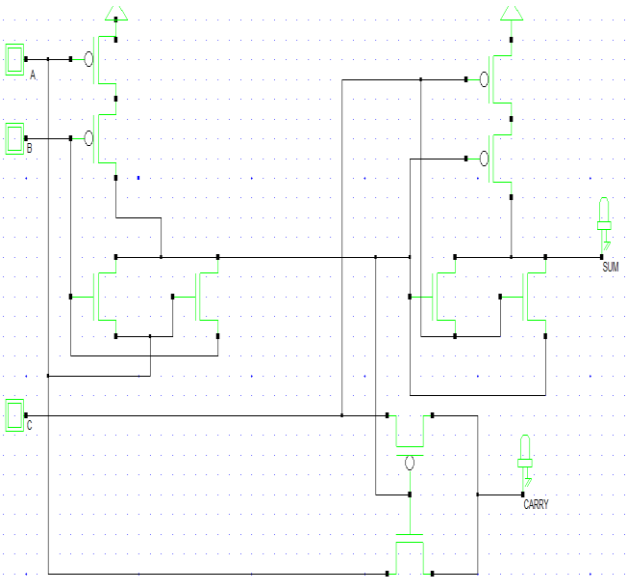

Figure 2 Architecture Design of 1-bit Full Adder using ten transistors

Energy efficient low power consumption full adder architecture has implement with the help of using CMOS transistor. In this paper, firstly design the 1-bit full adder circuit design in DSCH tool. Figure 3.2 represents the 1-bit full adder circuit using DSCH tool 2.7, in this design using ten transistor full adder circuits has been used to generate the Sum and Carry. The equations have been presented for 1-bit full adder circuit as given below to realize the architecture of 1-bit full adder design. This architecture of 1-bit full adder dissipated very little amount of power compared to base paper design. The equations for 1-bit full adder design are as follows.

$$Sum = A \text{ xor } B \text{ xor } CIN$$
$$Carry = AB + BCIN + CINA$$

In the presented low power full adder circuit the total number of transistors are less and all the transistors used are of minimum transistor sizes. Owing to the small electronic transistor sizes, low power consumption occurs across the transistor. There is less switch capacitance at the node once compare to the normal CMOS architecture, owing to the same size of the electronic transistor.

III. SIMULATION RESULT

Proposed Full adder with 10T is realized in circuit level with transistor resizing technique as shown in Figure III using DSCH designing software tool 2.7 and timing diagram shown in the figure IV. Layout level of this design is implemented in 90nm and 180nm technology using microwind tool 2.6 for delay evaluation as shown in figure V and figure VI respectively. Design is carried out in 90nm and 180nm technology to analyze the performance in technology scaling scenarios.

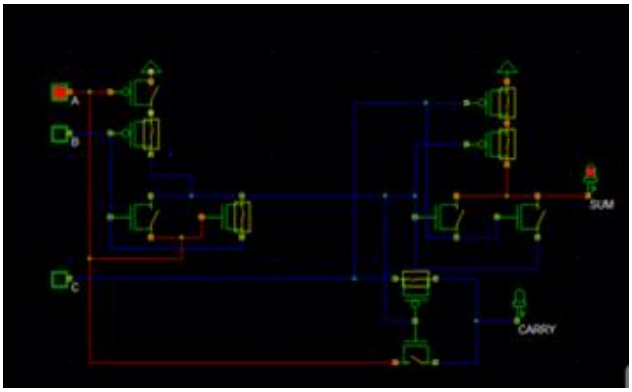

Figure 3 DSCH Full Adder Design.

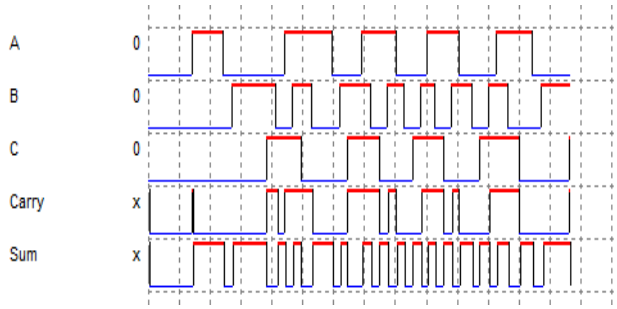

Figure 4 Timing Diagram of DSCH Full Adder Design Micro-Wind Result [(Proposed Design)]

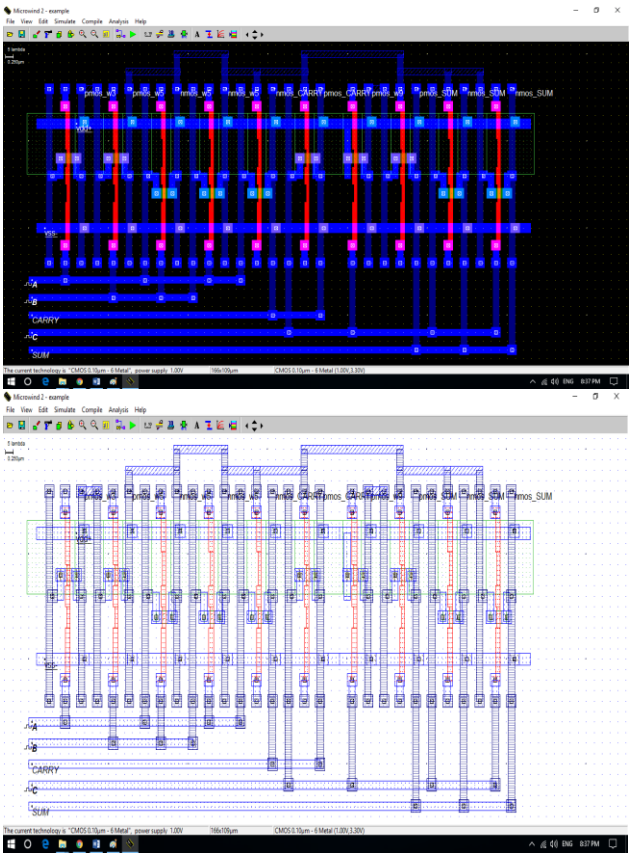

Figure 5 Layout of Proposed 1-Bit Full Adder Design in Micro-wind (90 nm).

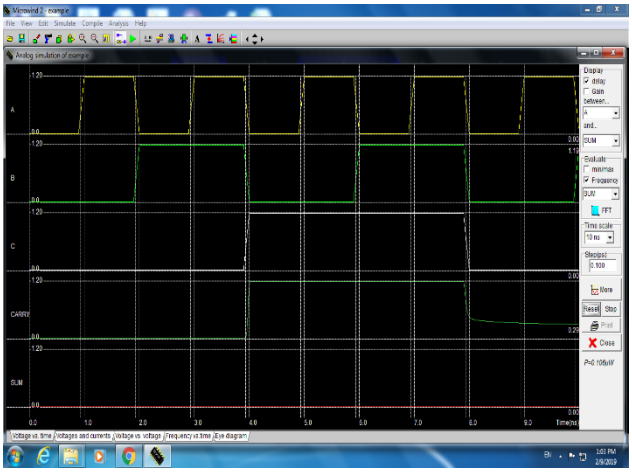

Figure 6 Results Waveform Voltage Vs Time of 1-Bit Proposed FA (90 nm).

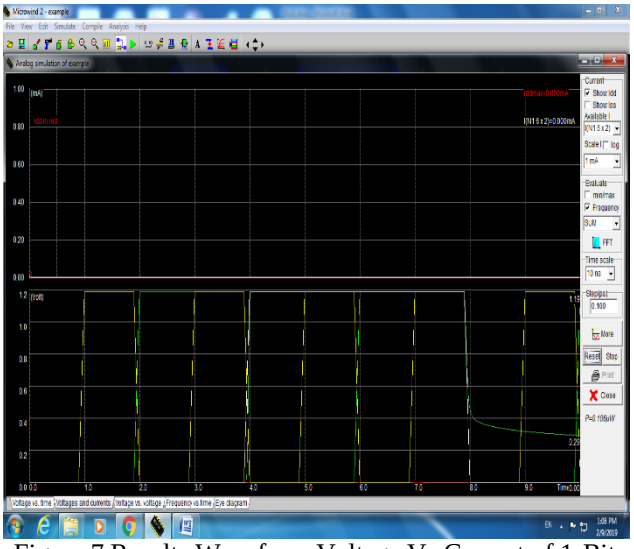

Figure 7 Results Waveform Voltage Vs Current of 1-Bit Proposed FA (90 nm).

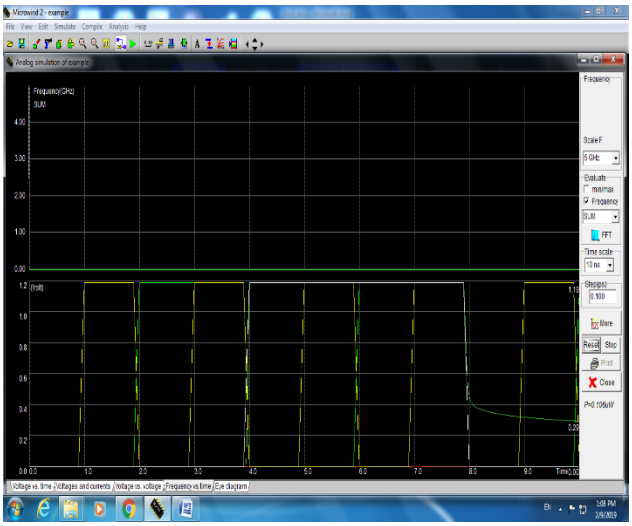

Figure 8 Results Waveform Frequency Vs Time of 1-Bit Proposed FA (90 nm).

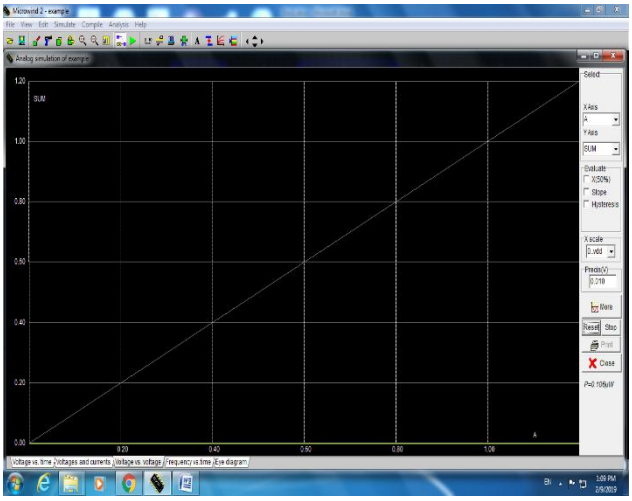

Figure 9 Results Waveform Voltage Vs Voltage of 1-Bit Proposed FA (90 nm).

In the figure 5 we show that the layout designs of proposed 1-bit full adder design which was generated in micro-wind layout tool. Figure 6 shows that the results waveform voltage Vs time of proposed 1-bit Full Adder Designing micro-wind. Figure 7 and 8 depicted the results waveform voltage vs. current of 1-bit Full Adder design and results waveform frequency vs. time of proposed 1-bit Full Adder design. The figure 9 depicted the results waveform voltage vs. current of 1-bit Full Adder design and results waveform voltage vs. voltage of proposed 1-bit Full Adder design.

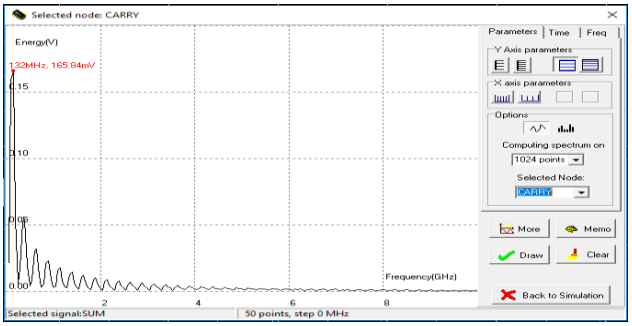

Figure 10 Shows the Fast Fourier Transform of pmos_carry of 1-Bit Proposed FA.

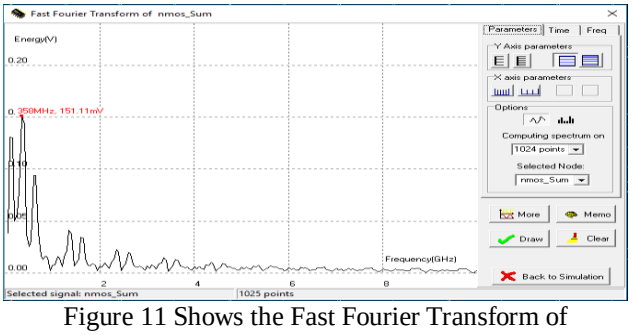

Figure 11 Shows the Fast Fourier Transform of nmos_sum of 1-Bit Proposed FA.

Figure 10 and 11 shows that the fast Fourier transform of NMOS sum and PMOS carry.

IV.CONCLUSION

In this paper we proposed 1-bit full adder design using ten transistors. This work employed 10 transistors to design low power high speed full adder. The circuit of low power full adder is designed by using DSCH tool 2.7 & analysis of the low power full adder design is done at room temperature in CMOS 90 nm technology by using microwind tool 2.6. In this work we minimizes the number of transistor & W/L is taken at 3:1 to reduce the power consumption & obtain high speed.

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