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Enhanced Performance Reversible ALU Design Using Reversible HNG Gate

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***Abstract*-ALU is the most essential block of any computer, microprocessor and digital signal processors DSPs. All the arithmetic and logical operations are performed inside the arithmetical and logic unit of the processor. The processing speed of the CPU is relying upon the complexity of the logics inside.Programmable reversible logic is developing as a prospective logic configuration style for execution in present day nanotechnology and quantum computing application with insignificant effect on generation of circuit heat. Late advancement in reversible logic utilizing and quantum computation algorithms take into account to enhance computers architecture and arithmetic logic unit architecture. The proposed ALU control unit configuration is made up from three Feynman reversible logic gates, three R-I reversible logic gates and one Fredkin reversible logic gate which is synthesized and simulated on Xilinx.14.7 ISE design suite. The simulation of proposed design has been done on Vertex-7 device family using Xilinx Isim HDL simulator. The obtained results are comparatively better as compared to existing results. The proposed design has quantum cost efficient. The quantum cost evaluated is "26n", has minimum garbage output evaluated "5n" and ancilla-input evaluated "3n+2" where "n" is the number of bits. With respect of device utilization, proposed design occupies less area reduced about to 12.86% and minimum aggregate evaluated delay is 5.96ns to achieve high- speed.**

***Keywords*-Arithmetic and Logic unit ALU, Reversible Logic gated, R-I gate, Fredkin gate, HNG gate.**

I.INTRODUCTION

One of the important parts of a digital computer is an arithmetic logic unit (ALU). ALU is designed to do the arithmetic and logic operations, including bit shifting operations which are the basic processes that need to be done for almost any data that is being processed by central processing unit (CPU). For most applications of all digital circuits, the two important attributes are maximizing speed and minimizing power consumption. The overall performance of the system will depend on the speed of the different modules used in the design.

CPU can be more powerful, but it also can consume more energy and creates more heat depending on how the ALU is designed. Therefore, it is important to balance between how powerful and complex the ALU is and how expensive the whole unit becomes. Faster CPUs are normally more expensive, consume more power and dissipate more heat.

There are many different power reducing techniques being used to design low power, high-performance chips based on complementary metal-oxide-semiconductor (CMOS) such as reducing voltage, load capacitance or switching frequency of the output node [1]. The most common and effective way of reducing the power consumption is by reducing the supply voltage (Vdd) which results in quadratic improvement in the power dissipation of a CMOS circuit

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity. The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation.

In this paper, we design a 1 bit reversible ALU that can perform twelve operations simultaneously. The 12 operations include addition, subtraction, multiplication, division, AND, OR, NOT and XOR. All the modules are simulated in ISIM and synthesized using Xilinx ISE 14.7. Further the proposed ALU has been extended by cascading up to 1024 bit.

II. BASIC REVERSIBLE GATES

Reversible logic gate are the device which has n×n inputs and outputs, its means input is equal to output or there is one to one mapping. Any gate is said to be reversible if the input can be recovered from the output. According to R.Landauer researcher there is power dissipation of KTln2 joules of heat energy per bit of information loss in classicalgates, where K is Boltzmann's constant and T the absolute temperature at which circuit performs [13].

1. Feynman Gate: It is a 2×2 reversible gate. A, B is input vector and P, Q is output vector. The output P=A, Q=A⊕B. It is used where copying is required and inverter both at the same time due to its output. The block diagram of this gate is shown in Fig .1

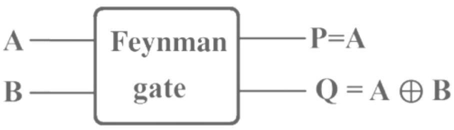

Figure 1 Feynman Gate.

Table 1 Truth Table of Feynman Gate.

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2. Fredkin Gate: It is 3×3 reversible logic gate having A,B,C as input vector and P,Q,R as output vector, where P=A,Q=A'B⊕AC , R=A'C⊕AB The block diagram of this gate is shown in Fig.2.

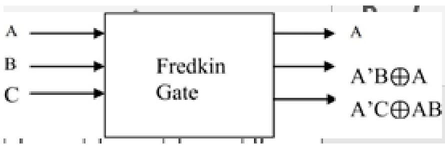

Figure 2 Block Diagram of Fredkin gate.

Table 2 Truth Table of Fredkin Gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

3. Peres Gate: It is 3×3 reversible logic gate. A, B, C is input vector and P, Q, R is output vector, where P = A, Q = A⊕B and R=AB⊕ C. The block diagram of this gate is shown in Fig.3.

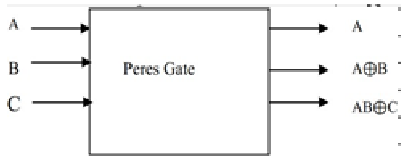

Figure 3 Block diagram of Peres gate.

Table 3Truth Table for Press gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	1	0

4. HNG Gate: It is a 4x4 gate and its logic circuit is as shown in the figure 2.4. It has quantum cost 6. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

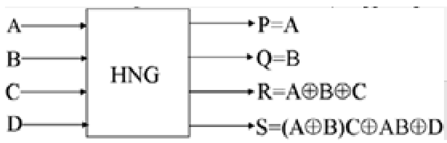

Figure 4 HNG Gate.

Table 4 Truth Table for HNG Gate.

Inputs				Outputs			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	1	0
1	1	1	1	1	0	1	1

5. R-I Gate: It is 3x3 reversible gate shown in Figure 2.5 which require only 7 transistors for transistor level implementation. RI gate is made of 1 xor, 1 or, 1 not and 3 and gates.

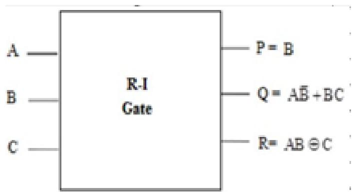

Figure 5 RI Block.

Table 5 Truth table for R-I

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	0

III. PROPOSED WORK

The proposed reversible ALU is designed to produce the same function as implemented by conventional ALU.Figure 6 is the block diagram of proposed reversible ALU designs. It has two main logic circuit design, namely,control unit and reversible full adder and the proposed design has five constants signals (e.g: Cinput1, Cinput2, Cinput3, Cinput4 and Cinput5) with a provision for realizing the eight arithmetic operations and four logic operations.

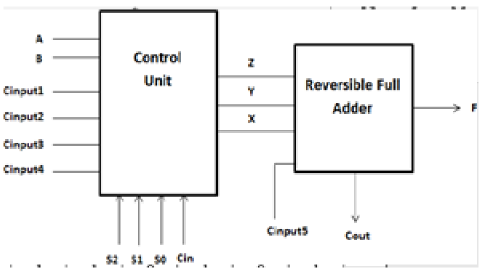

Figure 6 Proposed 1 Bit ALU.

1. Control Unit

Control unit is a critical part in the reversible ALU design. Control unit performs the arithmetic operations inside the ALU.

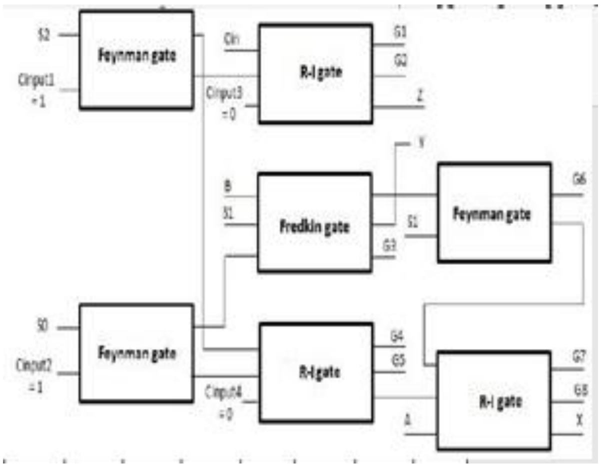

Figure 7 Internal Architecture of Control Unit.

As shown in Fig.7, the proposed control unit design is made up from three Feynman gates, three R-I gates and one Fredkin gate. Four control variables S2, S1, S0 and Cin select twelve different operations in the reversible ALU design. The arithmetic and logic operations are differentiated using the variable input of S2. The control unit has four constant signals. There are eight garbage outputs in the proposed control unit logic circuit.

Table 6 has given the operation code of proposed ALU architecture based on the combination of control line selection. Any specific operation can be performed with using a specific configuration of control line selection. Table has given total 12 operation out of them 8 operations are the arithmetic operation and rest of 4 are logical operations.

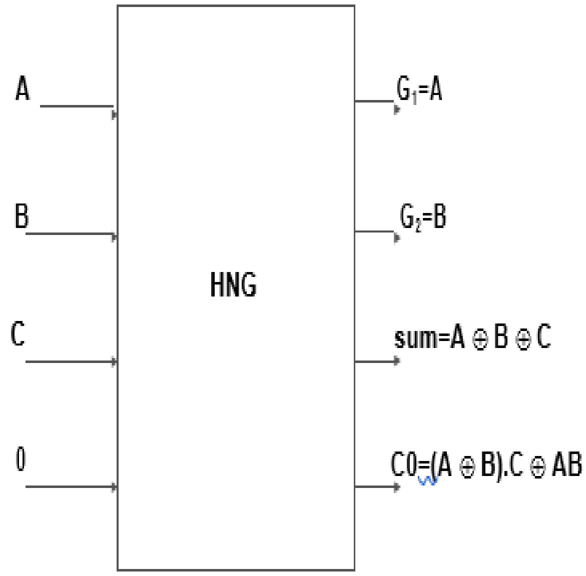

Figure 8 Full Adder Design Using HNG Gate.

In table function and their associated operations are given with respect of control line selection or based on select lines.

Table 6 Opcodes and Function.

SR.	S_2	S_1	S_0	C_{in}	Function	Operation
1	0	0	0	0	F=A	Transfer A
2	0	0	0	1	F=A+1	Increment A
3	0	0	1	0	F=A+B	Addition
4	0	0	1	1	F=A+B+1`	Add with carry
5	0	1	0	0	F=A+B’	Subtract with borrow
6	0	1	0	1	F=A+B’+1	Subtraction
7	0	1	1	0	F=A-1	Decrement
8	0	1	1	1	F=A	Transfer A
9	1	0	0	0	F=AorB	OR
10	1	0	0	1	F=AxorB	XOR
11	1	0	1	0	F=AandB	AND
12	1	0	1	1	F=A’	NAND

IV. SIMULATION OUTCOME

Simulation of proposed work has done Xilinx 14.7 ISE design Suite. Figure 9 has given implementation of proposed 1 bit ALU and internal architecture of proposed ALU has given in figure 10.

The technology schematic of proposed ALU has given in Figure 10. Further the design has implemented for 2 bit with cascading of two one bit ALU and 4 bit by using 2, 2- bit ALU and so on up to 1024 bit.

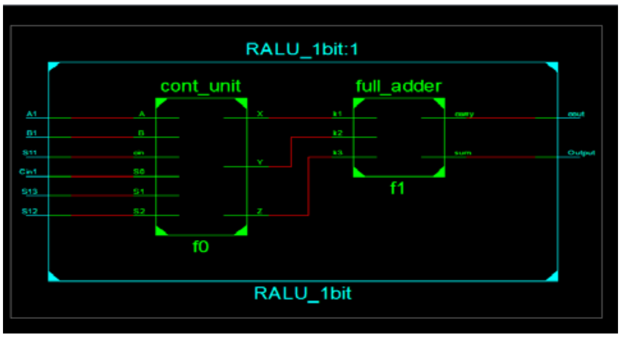

Figure 9 Proposed 1 bit ALU design.

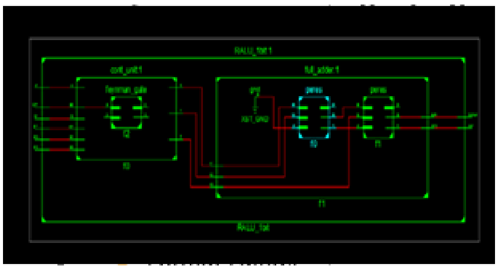

Figure 10 Internal architecture of proposed design.

Simulation of proposed design has done in Xilinx Isim HDL Simulator. Figure 11 and Figure 12 shows the simulation outcome of proposed design to perform two different ALU operations on different input vector.

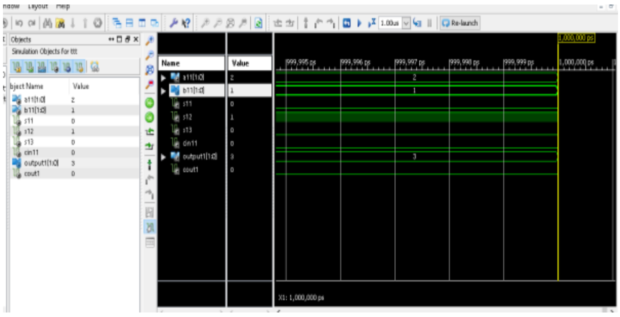

Figure 11 Simulation waveform 1.

Figure 12 Simulation waveform 2.

Table 9 has given the device utilization summary of proposed work based on area in terms of lookup table flip flops and speed in terms of critical path delay in nano second.

Table 7 Evaluated parameters on Xilinx Vertex 7 device family.

Parameter	LUTs	FF	IOBS	Delay
1-bit	2	2	8	1.044
2-bit	7	7	11	2.435
4-bit	8	8	16	3.478
8-bit	25	25	29	5.790
16-bit	49	49	53	10.440
32-bit	97	97	101	19.695
64-bit	193	193	197	38.205
128-bit	385	385	389	75.224
256-bit	769	769	773	140.260
512-bit	1537	1537	1541	297.261
1024-bit	3073	3073	3077	593.268

Table 8 Result Comparison Table 1

	Area (Slice)			Delay (ns)		
No. of Bits	PA_1[1]	PA_2[1]	Proposed Design	PA_1[1]	PA_2[1]	Proposed Design
n=2	9	9	7	2.67	2.61	2.435
n=4	16	16	8	3.88	3.78	3.478
n=8	30	30	25	6.12	5.98	5.790
n=16	59	58	49	11.77	11.05	10.440
n=32	111	108	97	22.61	21.07	19.695
n=64	212	208	193	42.02	41.49	38.205
n=128	397	393	385	81.78	81.04	75.224
n=256	788	783	769	153.78	151.05	140.260
n=512	1573	1566	1537	311.41	308.55	297.261
n=1024	3123	3113	3073	623.56	614.67	593.268

Table 9 Result Comparison table 2

Approach	AC	GO	QC
PA1[1]	(2n-1)	(3n+2)	35n+17
PA[2]	n	2n+3	34n+12
Proposed	5n	3n+2	28n

V. CONCLUSION

Reversible logic has promising application in the quantum computing. Reversible arithmetic units such as adders, subtractors, multipliers which form the essential component of a computing system have also been designed in binary as well as ternary logic. In recent years, researchers have emphasized finding reversible logic applications in promising emerging technologies. In past, several emerging technologies have been investigated for design exploration and application of reversible logic. In this work architecture of an efficient reversible ALU has been implemented and simulated on Xilinx 14.7 ISE design suite using VHDL hardware descriptive language. Fist a single bit ALU block has designed and then by cascading of two single bit reversible ALU a 2bit ALU has design has achieved similarly cascading of number of ALUSs a 1024 bit ALU has Achieved. The performance of proposed ALU has been evaluated based on Delay quantum cost and garbage output.

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