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Architecture of 8086 Microprocessor

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***Abstract* – The commercial design engineers primarily studied the 4004, 8008 and 8080 microprocessors for the needs of building control circuits and consumer products until 1971 to 1975. The introduction of the superior 8-bit 8085 microprocessor in 1976 drew the eye of the academicians who were charmed at the architecture and functionality of this chip and that they shortly included it as a course within the curriculum. As a result, the necessity for 8085 microprocessor Learning/Training System was a real demand and Intel released the SDK-85 Learning Kit without detailed design documentation. In 1978, Intel introduced the 16-bit 8086 microprocessor, which also found its place as a typical course at the tutorial institutions. Intel introduced the SDK-86 Kit for 8086 but once again without any detailed design information. The SDKs helped people learning the 8085/8086 architecture and programming but not knowing the planning methodology of a microprocessor learning system. The planning techniques remained within the realm of business companies. What's most astonishing thing about the massive success of the 8086, though, is how little people expected of it when it absolutely was first conceived. The history of this revolutionary processor could be a classic tale of what quantity a tiny low team of bright engineers can accomplish when they're given the liberty to try and do their jobs in innovative ways.**

***Keywords* – Intel 8086 microprocessor, Instruction Pointer, BIU.**

I. INTRODUCTION

Intel 8086 microprocessor is the enhance chronicle of Intel 8085 microprocessor. Intel was the mastermind for designing the 8086 microprocessor in 1976.

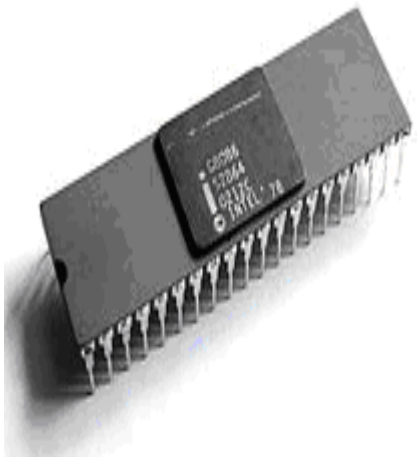
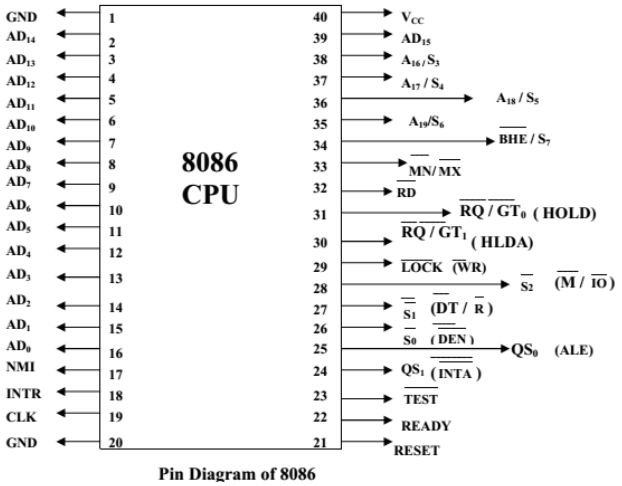


Fig. 1. 8086 Microprocessor.

The 8086 microprocessor is a 16 bit, N-Channel microprocessor. It is built on a single semiconductor chip and is a 40-pin IC. The type package is DIP (Dual Inline Package).
Intel 8086 has a 20-bit address bus and a 16-bit data bus. It can directly address up to 1M byte of memory. 8086 is designed to operate in two modes, i.e., Maximum and Minimum mode.



Pin Diagram of 8086

Fig.2.Pin Diagram of 8086.

II. INTERNAL ARCHITECTURE OF 8086

1. Microprocessor:

First we'd wish to debate some specific internal features, like its ALU, Flags, Registers, Instruction byte queue and segment registers. As shown within the subsequent diagram within the figure given below, the 8086 CPU is split into two independent functional parts, the Bus interface unit (BIU), and so the execution unit (EU). The processing accelerates by dividing the work between these two units. The BIU delivers addresses, retrieves instructions from memory, reads data from ports and memory and writes data to ports and memory. In other

words, the BIU handles all transfers of data and addresses on the busses for the execution unit. The Execution unit of the 8086 directs the BIU where ton deliver instructions or data from, decodes instructions and executes instructions.

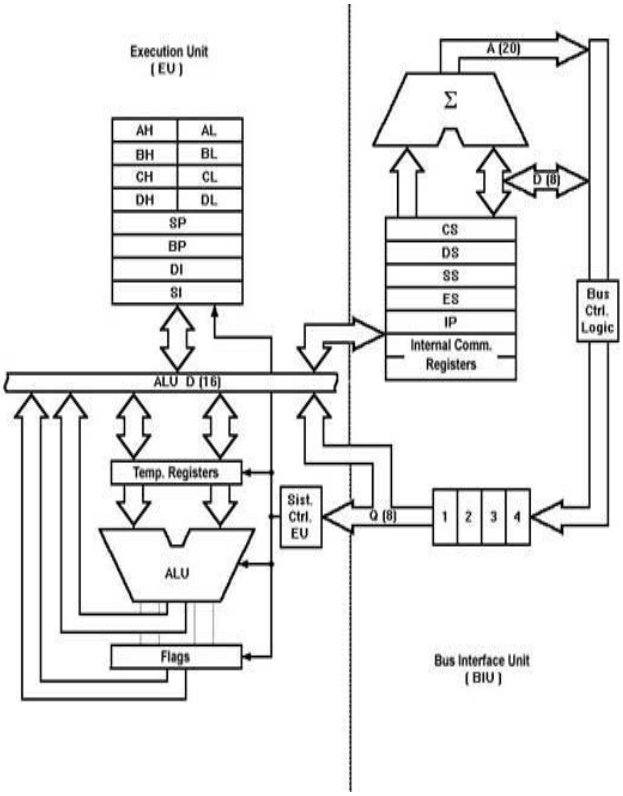


Fig. 3 .Internal Architecture of 8086 Microprocessor.

III. THE EXECUTION UNIT

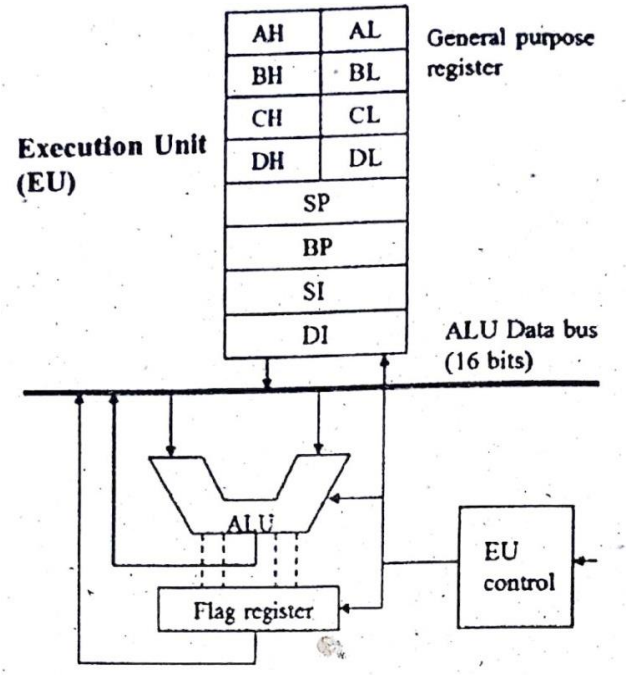


Fig.4.Execution unit.

1. Control Circuitry, Instruction Decoder, And ALU:

The EU contains control circuitry which handles internal operations. A decoder within the EU converts instructions fetched from memory into a list of actions which the EU carries out. The EU incorporates a 16-bit arithmetic and logical unit that may add, subtract, AND, OR, XOR, increment, decrement, complement, or shift binary numbers.

2. Flag Register:

A flag may be a flip flop that indicates some condition produced by the execution of an instruction or control certain operations of the EU. A 16-bit flag register within the EU contains nine active flags. From that nine flags six are wont to indicate. A 16-bit flag register within the EU contains nine active flags. From that nine flags six are wont to indicate some condition produced by an instruction. The EU, thus effectively runs up a flag' to inform you that a carry was produced.

The six conditional flags during this group are the parity flag (PF), the carry flag (CF), the Sign Flag (SF), the Auxiliary carry Flag (AF), the zero flag (ZF), and therefore the overflow flag (OF). The names of those flags should offer you hints on what conditions affect them. Certain 8086 instructions check these flags to work out which of two alternative actions should be worn out executing the instruction. The three remaining flags within the flag register are wont to control certain operations of the processor. These flags are different from the six conditional flags described above within the way they're set or reset. The six conditional Flags are set or reset by the EU supported the results of some arithmetic or operation. The control flags are studiously set or reset with precise instructions that you implant in your program. The three control flags are the trap flag (TF), which is employed for single-stepping through a program; the interrupt flag (IF), which is employed to permit or prohibit the interruption of a program; and therefore the direction flag (DF), which is employed with string instructions.

3. General Purpose Registers:

There are Eight general-purpose registers in the Execution Unit and they are labelled as AH, AL, BH, BL, CH, CL, DH, and DL. These registers will be used individually for the temporary storage of 8-bit data. The AL register is additionally called the accumulator. It's some features that the opposite general-purpose register doesn't have.

Certain pairs of those general-purpose registers will be used together to store 16-bit data words. the suitable register pairs are AH and AL, BH and BL, CH and CL, DH and DL. The AH-AL pair is observed because the AX register, the BH-BL pair is observed because the BX register, the CH-CL pair is observed because the CX register, the DH-DL pair is observed because of the DX register.

It was designed this fashion so the various programs are written for the 8086 or 8088. The advantage of using internal registers for the temporary storage of knowledge is that, since the info is already within the EU, it will be accessed rather more quickly than it may be accessed in external memory. Now let's take a glance at the features of BIU.

IV.BIU

1. Function of Segment Register:-

In 8086 complete 1MB memory is split into 16 logical segments. Each segment thus contains 64 KB of memory. While addressing any location within the memory bank, the Physical address is calculated from two parts, the primary part is the Segment address, and also the second is offset. The segment registers contain a 16-bit segment base addresses which are lump together with different segments. Thus the segment address for the Code, Data, Extra and Stack Segment is stored by the CS, DS, ES and SS segment registers. Each segment register contains a 16-bit base address that points to a very cheap addressed byte of that exact segment in memory.

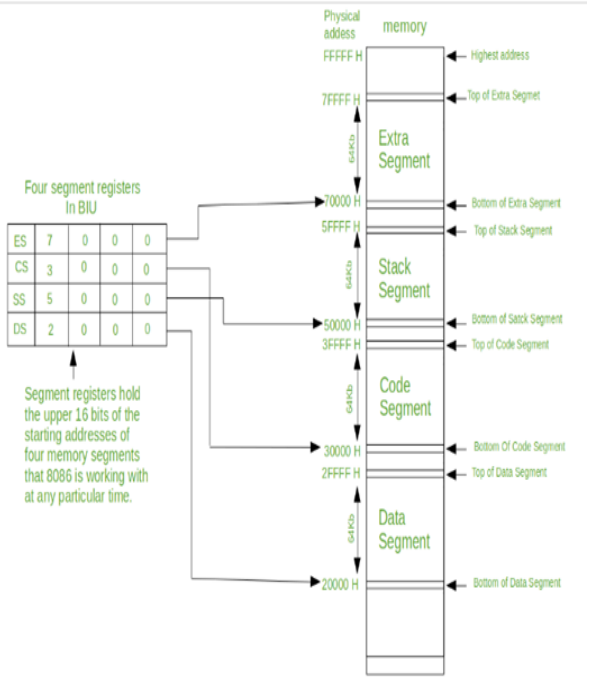


Fig .5. Segment Register .

2. The Queue

While the EU is decoding an instruction or executing an instruction that doesn't require the employment of the buses, the BIU fetches up to 6 instruction bytes for the subsequent instructions. The BIU stores these prefetched bytes in an exceedingly first-in-first-out register set called a queue. When the EU is prepared for its next instruction, it simply reads the instruction byte (s) for the instruction from the queue within the BIU. This is often much faster than sending out an address to the system memory and anticipating memory to challenge the following instruction byte or bytes.

3. Segment Registers:

BIU has 4 segment buses, i.e. CS, DS, SS & ES. It holds the addresses of instructions and data in memory, which are employed by the processor to access memory locations. It also contains 1 pointer register IP, which holds the address of the following instruction to execute by the EU.

CS − It stands for Code Segment. it's used for addressing a memory location within the code segment of the memory, where the executable program is stored.
DS − It stands for Data Segment. It consists of information employed by the program and is accessed within the data segment by an offset address or the information of another register that keeps the offset address.

SS/ES − It stands for Stack Segment. During execution it controls memory to store data and addresses. ES it stands for Extra Segment. ES is a further data segment, which is employed by the string to carry the additional destination data.

4. Stack segment register and stack pointer register:

In 8086, the main stack register is known to be stack pointer-SP. The stack segment register (SS) is usually used to stock information about the memory segment that stores the call stack of currently executed program. SP points to current stack top. Inadequately the stack grows downward in memory, so newer values are arranged at lower memory addresses. To put a value in the stack, a push instruction is used.

5. Instruction Pointer:

The 8086 uses the register CS and IP to access the instruction. The CS register contains the segment number of the subsequent instruction and IP contains the offset. In spite of other registers the IP cannot directly be manipulated by instruction, that is, an instruction might not contain IP as its operands. It is a 16-bit register. It holds the offset of the subsequent instructions within the Code Segment. After every instruction byte is produced, the IP is incremented. IP gets a brand new value whenever a branch instruction occurs. CS is multiplied by 10H to provide the 20-bit physical address of the Code Segment. The address of the subsequent instruction is calculated as CS x 10H + IP.

V. CONCLUSION

8086 Contains Two Independent Functional Units 1) Bus Interface 2) Execution Unit. The BIU handles transfer of data and addresses between the processor and memory devices. The EU receives opcode of an instrument from the queue, decodes it and then executes it.Now

microprocessor become one of the most significant inventions to technology. It is used in different aspect of life it can store larger data then the size of actual chip.

VI. ACKNOWLEDGMENT

I have great pleasure in presenting the report on "An overview of Architecture of 8086 Microprocessor". I take this chance to precise my sincere due to my guide Prof. Rohini B. Jadhao class in charge of the Department of Electronics Engineering, S.L.R.T.C.E., Mumbai, for providing the technical guidance and therefore the suggestions regarding the work. I'd wish to express my gratitude towards their constant encouragement, support and guidance throughout the event of the report.

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