International Journal of Scientific Research & Engineering Trends
Volume 5, Issue6, Nov-Dec-2019, ISSN (Online): 2395-566X

A Survey on Low Power High Speed Domino Circuit in Low Power VLSI Design

MD Naushad Akhtar
Dept. of ECE, RNTU, Bhopal,
mdnaushad.akhtar@gmail.com

Ashish Chouhan
Dept. of ECE, RNTU, Bhopal,
mdnaushad.akhtar@gmail.com

Priya Kumari
Dept. of ECE, RNTU, Bhopal,
mdnaushad.akhtar@gmail.com

***Abstract* - Increased number of transistor count and reduced device size is main reason behind scaling and this incorporates leakage current also in other hand battery technology is growing very slowly hence we need low power circuit so that we can enhance overall performance of device. After evolution of CMOS circuit the scientist moved on static and dynamic circuit design. In static CMOS there are various limitations like no. of transistor count, power dissipation, slow speed, hence to overcome these limitation a new circuit pseudo NMOS is used. It exist somewhere between static and dynamic circuit. We have seen that FinFET technology is simulated by BISM4 model using HSPICE at 32nm process technology at 250C with CL=1pF at 100MHz frequency. When CMOS is compared with FinFET for 8 and 16 input OR gate we save average power 15.46%, 21.34% SFLD, 57.37%, 20.12% HSD, 30.90%, 42.46% CKD respectively.**

***Keywords* - FinFET, High Speed, shorter channel effect, Multigate device.**

I. INTRODUCTION

Dynamic circuit is similar to sequential circuit with memory function. Dynamic circuit used widely, since it provides less delay, lower power dissipation and reduced area in comparison of static circuit design. Domino circuit design is a type of dynamic logic which is used where high performance is the prime requirement. Domino logic CMOS circuit allows significant reduction in number of transistor count. It also a good combination where fan-in of the domino circuit is high are high such as multiplexer or comparator circuit.

Main goal of Very Large Scale Integration (VLSI) circuit design is to integrate more number of transistor, more no of logic gates, area reduction. Area reduction can be done in three different ways
(i) using advance processing technology like scaling.
(ii) Circuit design technique.
(iii) Careful chip layout. In designing of high performance low power VLSI circuit power consumption and gate delay are crucial elements. In nanoscale static power dissipation is of considerable amount. Domino circuit used widely in memory[14-15],due to using parasitic capacitances as charge storing element, multiplexer[16], comparator, due to providing facility of wide fan in, [18] and arithmetic circuit [19-22] and also used in full adders that are most important component of Centre Processing Unit (CPU).

Domino logic is used for implementing any Boolean logic function or circuit it gives several benefits in terms of delay size and power etc. in modern digital design when we are talking about large no of transistor count that are used in fabrication of a chip the yields are considerable. But leakage and low capability to avoid the noise in the circuit is a big deal in case of domino logic.

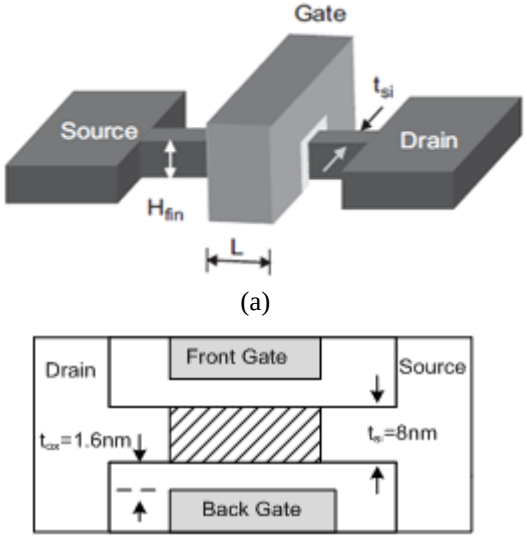

Fig. 1. (a) FinFET 3D View of one Fin. (b) Top view of FinFET.

1.Research Objective and Problem Formulation

Introduction of technique (Domino circuit) that can help in reduction of leakage power. Find different domino circuit that can be used as diode switch and also help in reduce contention current in dynamic circuits. As the switching activity increase power consumption in dynamic circuit also increases. Study the previous techniques to minimise the redundant switching and

develops some new design techniques.Simulate and compare proposed domino circuit with standard domino circuit. Where comparison should be in terms of power consumption speed and noise immunity.

II. FINFET TECHNOLOGY

In FinFET is a device which is constructed in the three dimensional view in which channel is formed while wrapping around the thin insulator for the formation of channel. For the formation of FinFET device, a thin vertical layer which is called Fin which is the shape of fish of fines over the silicon substrate. The thin layer of the fines which is forming as source and drain terminal of the transistor. The wrapping of thin layer over the gate terminal from two or more sides. Which is having the good control over the channel from two or more sides? As the shape of this fin has good control which can operate one transistor in active region. FinFETs technology is better substitute to CMOS technology in order to suppress the shorter channel effects.

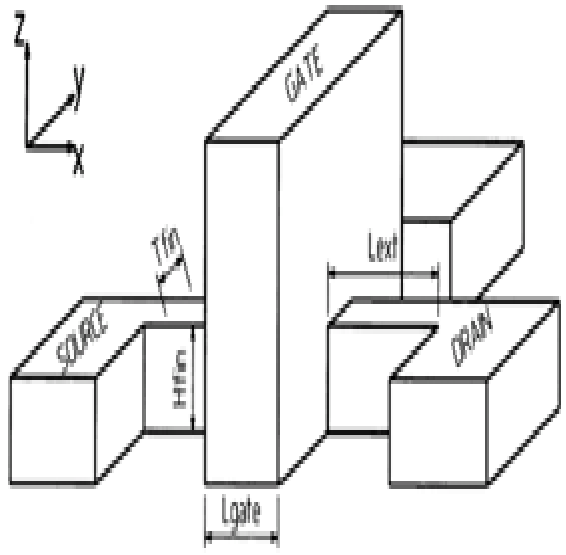

Fig.2. FinFET structure.

Due to vertical gate structure finFET width is quantized, Fin hight is determine by minimum transistor width (W_{min}). With the two gates of a single-finFET tied together, W_{min} is Effective channel width

$$W_{min} = 2 \times H_{fin} + t_{fin}$$

Effective channel length $L_{eff} = L_{gate} + 2 \times L_{ext}$

where H_{fin} is the height of the fin and t_{fin} is the thickness of the silicon body L_{ext} is the extension of fin from gate to source or drain terminal[4]. In order to suppress shorter channel effect and enhance the area efficiency in FinFET, fin thickness is much smaller than fin height[5-7].

Table I: Device Technology Parameters

Parameter	32nm N-FinFET	32nm P-FinFET
Length of Channel (L)	32nm	32nm
Fin thickness(t_{si})	8.6nm	8.6nm
Fin height(H_{fin})	40nm	50nm
Oxide thickness(t_{ox})	1.4nm	1.4nm
Source/drain doping(N-type and P-type FinFETs)	$2x10^{-20}$ cm^{-3}	$2x10^{-20}$ cm^{-3}
Power Supply (V_{dd})	0.8V	0.8V

To suppress Short Channel Effects (SCE) (arose due to aggressive scaling) and leakage current also to enhance performance a gate control over channel is required. This is achieved by multi gate Field effect transistor (FET) known as FinFET. Vertical channel structures (gates) which resembles like fins of fish are used in FinFET channel is formed perpendicular to the wafer plane and current flow parallel in the FinFET transistor as shown in Fig.2 [16, 17]. The shape of the fins is such a way that it is lightly doped or undoped, which help in improvement of carrier mobility of the charge carriers and suppression in doping fluctuation in a Double Gate (DG) compared with MOS technology[18].

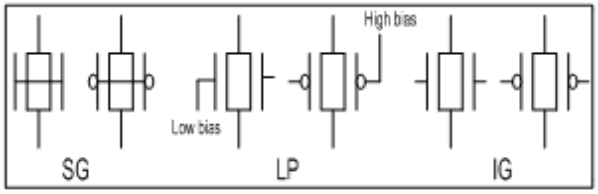

Fig. 3. Mode of operation of FinFET.

Variety of circuits are presented here that deal with low leakage better noise handling and have wide fan-in. These circuits suggest various techniques, like when we are comparing the measured switching current of the ON transistors in active region and leakage currents of the OFF transistor to control the PMOS charge keeper transistor, provide reduced contention current among pull down network, keeper transistor and dynamic node. To suppress the leakage current for the improvement of overall performance of current mirror stacking effect is used.

Gaetano Palumbo et.al; [1] describes "A new circuit approach to increasing the speed of the circuit there is a technique is introduce known as Domino logic gates" for less delay variability as compare to the conventional circuit a new approach is described which makes a new circuit. The circuit have two keeper transistor the main authors of this paper is to reduce the delay variability by decreasing the loop gain including feedback.

Massimo Alioto et.al; [2] titled "For measuring the different parameters like process variation on different device parameters and Domino logic" explains about two different process named as inter-die and intra-die process variation and it affects the circuit. This paper also explains about sizing, fan-in and fan-out. Due to variation in current it shows delay variation delivered by logic gates and variation of parasitic capacitance is negligible in entire process.

Ali Peiravi et.al; [3] In this paper it shows different domino logic circuits performance parameters for the robustness of the circuit. A new controlled keeper by current comparison domino CKCCD which is a leakage and noise tolerant domino logic circuit is explained in this paper. Due to the low level input and the current, at least one input at high level, the keeper is controlled to reduce contention current and get a high performance through the current comparison.

A.Kabbani et.al; [4] In this paper author has improved the noise immunity of the circuit in wide Fan in gates in domino circuits. To determine response of a dynamic CMOS logic the amplitude and width of noise pulse play an important role. In this paper, a mathematical model is presented for determination of noise in dynamic logic CMOS circuit. For both long channel and short channel MOSFET these analysis is done here.

Mohammad Asyaei [5] In this paper author compare the voltage of wide fan-in gates in deep sub-micron technology for the measurement of low power consumption and higher power immunity without significant delay for wide fan-in gate is achieved using a new leakage tolerant circuit. The idea behind the proposed circuit is taking in to consideration of sense amplifier for sensing the difference between the voltages across the pull down network.

Table II: Results of I_{OFF} & I_{ON} of 4T P-FinFET for single Fin

V_{BG}	I_{OFF}(aA)	I_{ON} (µA)
0.2	386.5	7.52
0.3	242.3	6.37
0.4	21.02	4.45
0.5	4.57	3.31
0.6	263	2.45
0.7	1.52	0.94

Table III: Results of I_{OFF} & I_{ON} of 4T N-FinFET for single Fin

V_{BG}	I_{OFF}(pA)	I_{ON} (µA)
-0.2	0.073	0.921
-0.3	0.352	11.20
-0.4	3.163	12.63
0.0	33.32	17.31
0.2	73.36	18.42
0.4	3421	20.12

III. LITERATURE REVIEW

Domino logic circuit is basically used in high speed microprocessors, where speed and high performance is the prime concern with scaling of technology.

1. Footless Domino Logic Circuit

In dynamic CMOS, parasitic capacitances are used in fruitful manner, circuit are realized using the parasitic capacitors to store information. This is also done in memory. Dynamic CMOS circuit provide high performance circuit. Even providing faster speed and less area it suffers from different other problem like charge sharing, power dissipation because of switching activity, glitch power etc. unlike static CMOS, dynamic circuit consist a clock. Clock is connected to both PUN and PDN circuit that is a PMOS and a NMOS and required circuit is designed using NMOS clock is used to differentiate between recharge and evaluate phase as shown in Fig. 4.

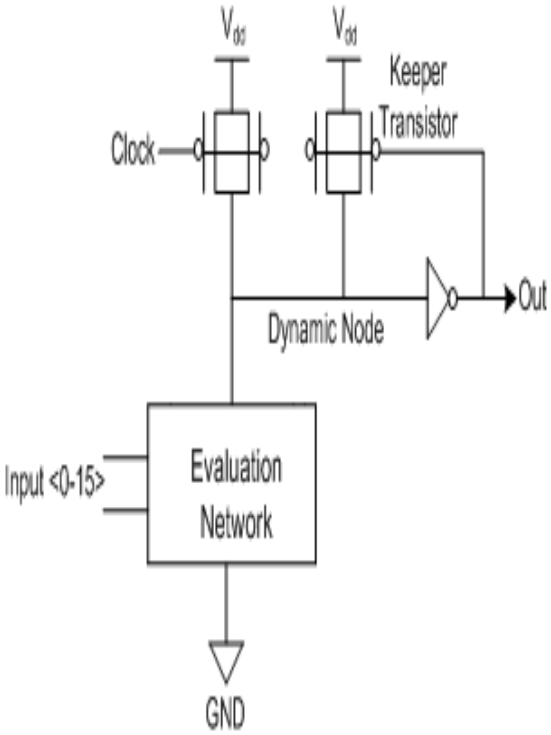

Fig. 4. Footless domino logic circuit.

2. Footed Domino Logic Circuit

The clock is nothing but a continues pulse train when the clock is low it is called recharge phase during this period PMOS is on and NMOS (connected with clock) is off hence load capacitance is charged to Vdd or we can say that dynamic node is charged now when clock is high or we can say ,in evaluation phase PMOS is off and NMOS is on hence provide a path to ground now depending on input to NMOS circuit the output start getting discharge recharge given as shown in Fig. 5.

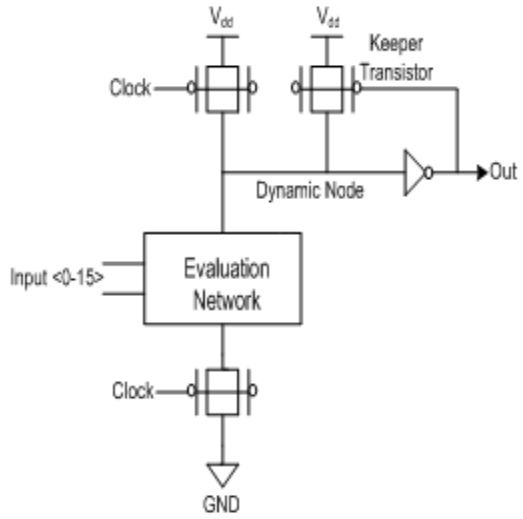

Fig. 5: Footed domino logic circuit.

3. High speed Domino Logic Circuit

Due to the extra clock delay, it consumes extra area and power which is the demerit of the circuit. It gives an effective solution to increase the robustness of the circuit. When clock becomes high In High speed domino logic circuit M_{p2} is still on and, M_{n1} is still off. During the evaluation phase if dynamic node remains high NMOS is turn on which turns on the keeper transistor. Therefore at the starting of the evaluation phase dynamic node is afloat, when the keeper transistor is not present, at the input section dynamic node may be discharge for any noise. [9].

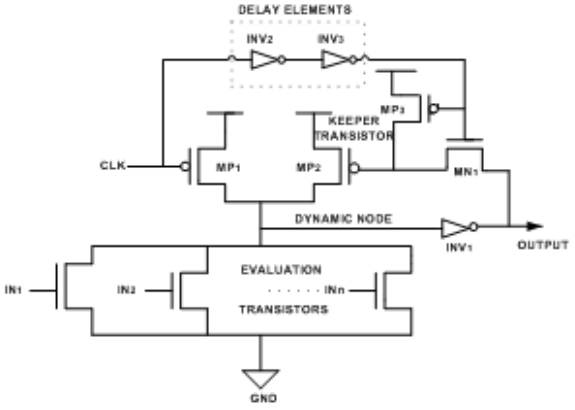

Fig. 6: High speed domino logic circuit.

4. Conditional keeper Domino Logic Circuit

This will form transmission gates at the upper part and reduce the effective resistance on charging time. The difference lies in the lower part where an additional power clock is used and an extra NMOS and PMOS are implemented. The drain and gate of NMOS are shorted together, which makes it act as a diode. Hence at the output of the gate noise and leakage exists for a long time unnecessarily.

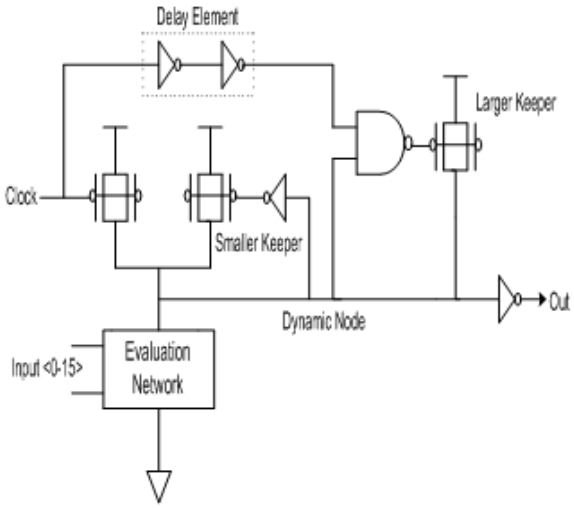

Fig. 7. Conditional keeper domino logic circuit.

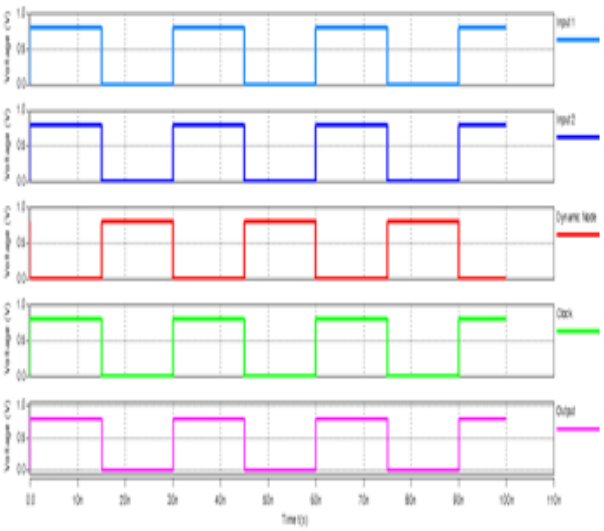

Fig. 8. Transient characteristics of 2-input Domino OR using HSPICE in FinFET technology.

V. SIMULATION AND RESULTS DISCUSSION

The existing and proposed domino circuit techniques are implemented in the FinFET and CMOS technologies. For gating the fair comparison of the results we simulated the existing and proposed circuit at same at 32nm of process technology with the help of BPTM library 0.9V of supply voltage, output capacitance of the circuit is taken as C_L=1pF and. For the noise-tolerance measurement, the UNG noise pulse width 50 ps (higher than the gate delays) is taken and the noise-voltages are applied to all the inputs. Average power, Delay, power-delay product (PDP), evaluation delay and standby power for the different schemes of the OR gate with the fan-in gates 8 and 16 inputs are shown in TABLES I and II gate (n-type CMOS and FinFET: W/L =1, p-type

CMOS and FinFET: W/L = 2). Table III shows the comparison of the UNG with the existing and proposed circuits for the 8 and 16 inputs in CMOS and FinFET. In Table IV when the transistor width is doubled (n-type CMOS and FinFET: W/L =2, p-type CMOS and FinFET: W/L =4) there increase in the power consumption of the device, delay of the network is measured and saves the averaged power consumption of 18.37%, 30.12% SFLD technique, 45.67%, 42.84% HSD techniques, 52.43%, 54.72% CKD techniques.

	8 INPUT OR GATE		
Topology	Avg. Power(uW)	Delay(pS)	UNG
FDL	0.662	17.99	0.242
FLDL	0.568	11.91	0.204
CKD	0.846	24.45	0.326
HSD	0.676	8.492	0.248
LCR	0.963	10.99	0.263
DFD	0.921	17.13	0.236

Table IV: CMOS existing Domino for 8 input OR Gate

	16 INPUT OR GATE		
Topology	Avg. Power(uW)	Delay(pS)	UNG
FDL	0.912	21.42	0.218
FLDL	0.670	12.82	0.221
CKD	1.142	31.46	0.395
HSD	0.912	13.54	0.243
LCR	1.173	16.43	0.264
DFD	1.109	25.74	0.223

Table V: CMOS existing Domino for 16 input OR Gate

	Average Power		Delay		PDP	
	SP Mode	LP Mode	SP Mode	LP Mode	SP Mode	LP Mode
FLD	0.1200	0.0316	9.635	8.243	1.156	0.2608
FDL	0.0776	0.0242	15.58	13.45	0.492	0.0119
HSD	0.1306	0.0342	9.185	7.982	1.199	0.3987
CKD	0.1537	0.0428	10.32	9.541	1.586	0.4083

Table VI: Calculation of Average power, Delay and PDP for 8 input OR gate in SP and LP mode using FinFET technology.

	Average Power		Delay		PDP	
	SP Mode	LP Mode	SP Mode	LP Mode	SP Mode	LP Mode
FLD	0.142	0.038	10.23	9.371	1.461	0.364
FDL	0.096	0.027	19.94	15.34	1.914	0.426
HSD	0.157	0.039	10.02	9.254	1.460	0.362
CKD	0.183	0.049	11.01	10.25	1.883	0.506

Table VII: Calculation of Average power, Delay and PDP for16 input OR gate in SP and LP mode using FinFET technology

VI. CONCLUSION

FinFET based LPS Domino circuit design saving the average power consumption of 18.37%, 30.12% SFLD technique, 45.67%, 42.84% HSD techniques, 52.43%, 54.72% CKD techniques, 31.35%, 44.34% DFD and when compared with MOS based proposed techniques it saving the average power of 11.72%, 21.34% SFLD, 38.63%, 38.73% HSD, 96.23%, 94.43% CKD, 18.36%, 24.83% LCR, 14.12%, 15.42% DFD which is shown for the 8 and 16 input OR gates, respectively. In Table II it is also observed that the UNG for the 8 and 16 input OR gates in the MOS is quite high compared with that of the FinFET technology in the existing and proposed circuits because of the three-dimensional structure of the FinFET and the great number of fringing and overlapping capacitance associated with it, in which the shorter length of the channel and gate current is dominant in the FinFET compared with the MOS.

REFERENCES

[1]. International Technology Roadmap for Semiconductors (ITRS) 2001, 2002, Courtesy.
[2]. Moore‟s Law meets static power, Computer, December 2003, IEEE Computer Society.
[3]. S.M. Kang and Y. Lablebici, “CMOS Digital Integrated Circuits: Analysis and Design”, 3rd Edition Tata Mc-Graw Hill, 2003.
[4]. A.P. Chandrakasan et al. “Low- power CMOS digital design”, IEEE Journal of Solid-State Circuits, Vol.27, no.4, pp. 473–484, Apr. 1992.
[5]. J. M. Rabaey and M. Pedram, “Low Power Design Methodologies”, Kluwer Academic Publishers, 1996.
[6]. G. Karimi, A. Alimoradi, “Multi-purpose technique to decrease leakage power in VLSI circuits”, Canadian Journal on Electrical and Electronics Engineering, Vol.2, no.3, pp.71–74, 2011
[7]. W. Hisamoto, W.C. Lee, J. Kedzierski et al. “FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm” IEEE Transaction on Electron Devices, Vol.48, no.10, pp. 2357–2362, Oct. 2001.

[8]. S. Borkar, "Low power design challenges for the decade", in Proceedings of the EEE/ACM Asia and South Pacific Design Automation Conference, pp.293–296, June 2001.

[9]. S.A. Tawfika, and V. Kursun, "FinFET domino logic with independent gate keepers", Microelectronics Journal, Elsevier, Vol.40, pp.1531-1540, 2009.

[10]. P. Mishra, A. Muttreja, N. K. Jha, "FinFET Circuit Design, SPRINGER",Nanoelectronic Circuit Design, DOI 10.1007/978-1-4419-7609-3_2, pp. 23-53, 2011.