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A Survey on Different Adiabatic Logic Circuits for Low Power in Dsm Technology

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***Abstract* - The term 'adiabatic' is coined from thermodynamics in which a method where no energy exchange takes place with environment results no dissipation of energy loss. On the other hand in short circuit devices in energy exchange process charge has been transfer between different nodes. Practically, with the use of partial adiabatic operation in the circuit results for the improvement of overall performance of the circuit with complexity. The result is represented in tabular and graphical form. And a comparison is done among all the simulation. After a detailed examination a conclusion has been drawn based on the entire work done and also from the simulation and the result is evaluated. All simulations are carried out using HSPICE at 65nm technology with supply voltage is 1V at 100MHz frequency, for fair comparison of results W/L ratio of all the circuit is same.**

***Keywords*-Low power, Adiabatic logic, ECRL, 2N-2N2P, PFAL.**

I. INTRODUCTION

The size of the conventional CMOS circuit is reduced upto its zenith. When the scaling of the technology takes place to improve the result, all the technology which are further developed is trying to mitigate the leakage power. In DSM technology power consumption can be done in the form of static CMOS circuit design, if it is happen energy loss is taking place with scaling of technology due the charging and discharging of the PDN and PUN of the CMOS transistor.

Due to this the motivation to reducing the dynamic power in the CMOS circuit takes place, one of the technique is adiabatic logic. In conventional CMOS circuit design the PUN in load capacitors from VDD and dissipate the charge store in the capacitor through PDN towards GND. In the adiabatic logic circuits, Which prevents the discharging of the energy through the GND and energy is reused. It also avoids the instant charging and dis charging of the output capacitance in CMOS circuits, in adiabatic switching operation of the nodes are charged and discharged at a constant rate which results into a further power reduction in the circuit.

The adiabatic logic is now proving to be a better selection to other conventional circuit, because it is an emerging circuit design technology, it has a lot of scope available in the research field. [1-3]. A huge work is constructed with mitigation of overall power consumption of the circuit. And different pattern of adiabatic logics are available which have its own advantages and disadvantages with the others, but still lot of researches are going on which shows there a huge scope for our research. After analyzing the literature we find that there are many adiabatic logic circuits have been given so far. A brief look is given as under.

J. S. Denker et.al. [1]: This paper describes the fundamentals of the adiabatic computing principle. It includes the motives and objectives that why the low energy computing is important. This paper shows the compulsory energy loss of $\mathbf{0.5}\boldsymbol{CV_{dd}^2}$ during charging and discharging process of the CMOS circuit and then explains how the adiabatic logic is recovered the energy loss in the circuit and provides low power dissipation [7-9].

S. Hemantha et.al. [2]: This paper explains multi-threshold CMOS designs for achieving low power in VLSI circuit. Power gating transistor is connected between the power supply or GND and logic transistor in multi-threshold CMOS, therefore it creates either a virtual supply rail or a virtual ground rail respectively. For achieving low leakage current MTCMOS technology is helpful by utilizing high threshold voltage (Vt) sleep transistors an with the help of low v_t transistor high performance can be achieved. In this paper the author has successfully reduced the delay of power gated circuits during active mode of operation. It is done by reducing the voltage drop across the sleep transistor.

Y. Moon et.al. [3]: In the given paper efficient charge recovery logic (ECRL) circuit is proposed. In this circuit the two PMOS transistor are forming a latch as a pull up network on the other hand two NMOS transistor are attached in pull down manner, forming the logic which

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is implemented. The ECRL logic is explained in detailed manner in this paper.

A. Kramer et.al. [4]: In this paper author has given a new type of adiabatic circuit which has various advantages over other. The author has represented the second order adiabatic circuit like 2N2P and 2N-2N2P adiabatic logic circuits. The principle which is used in adiabatic charging is explained in detailed as well as energy dissipation calculations. The four phase trapezoidal clock has been discussed along-with the four phase of its operation. By analyzing the simulation of the circuit the author came to know that the 2N-2N2P.

II. CONVENTIONAL CMOS AND ADIABATIC LOGIC

The term Adiabatic is taken from thermodynamics which mean there is no exchange of energy with the environment, hence no energy dissipation loss takes place. In this process no gain or loss energy takes place and thus no change in entropy in the quasi-state approximation, whereas in semi-conductor devices in the process of energy exchange the charge has been transferred between different nodes so the different techniques are used to minimize the energy loss due to charge transfer process. In this area of research the reversible logic has been mainly used so as to circuit getting smaller and faster continuously, energy dissipation increases tremendously. This problem can be solved by designing the circuit using principle of thermodynamic process called Adiabatic Process. So the designer implements adiabatic process.

For saving of power consumption, Adiabatic logic are basically used CMOS technology. CMOS technology has more weight age than other technology available. During switching activities in CMOS most of the energy is wastes in the form of heat. There two basic principle which has been followed in any Adiabatic logic

1. During simulation it is found that difference in the voltage between the drain terminal and the source terminal a transistor should never be turned on.
2. In the transistor current flowing through is opposes it should never be turned off the device of the transistor.

1. Adiabatic LOGIC

The above diagram shows a simple inverter/ buffer implemented using fully adiabatic logic. In between the two transmission gates Pulsed power supply **'pck'** is applied. On the left side is implementing the inverter function with its output as **fbar** and other one is driving the buffer function with output **f.** With the help of dual rail outputs both the positive and negative function can be achieved simultaneously. This adiabatic logic circuit will be much energy efficient and dynamic power dissipation can be reduced drastically if the power supply is design in such a way that the energy can be recovered. In previous works [11], different type of fully adiabatic logic like SCRL (Split Charge Recovery Logic), PAL (Pass Transistor Adiabatic Logic) has been presented [12].

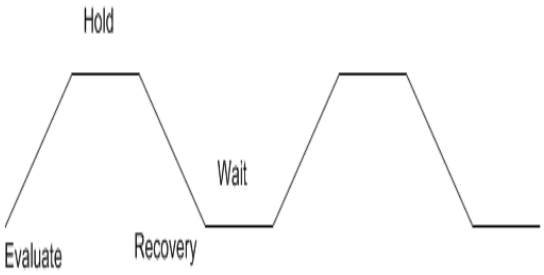

Fig.1. Four Phased Trapezoidal Power Clock.

2. Efficient Charge Recovery Logic (Ecrl)

Efficient Charge Recovery Logic (ECRL) [5], as shown in Fig. 2, uses two cross-coupled PMOS transistors and two NMOS transistors in the N-functional blocks of ECRL logic block. In order to recover and reutilize the supplied energy, ECRL gates uses AC power clock (pck). Let us assume **In** is at high and **Inb** is at low. At the beginning of a cycle, when power clock 'pck' rises from zero to VDD, **Out** remains at low level because the high input **In** turns the F NMOS logic high. Output **Outb** follows the power clock 'pck' through M1. Now when 'pck' reaches to VDD, the outputs hold valid logic values. During the hold phase these output values are maintained and can be used as inputs for evaluation of next stage. In the next phase of recovery, the power clock falls down to zero level and the energy from the output node can be returned to the 'pck' so as to recover the delivered charge [13-16].

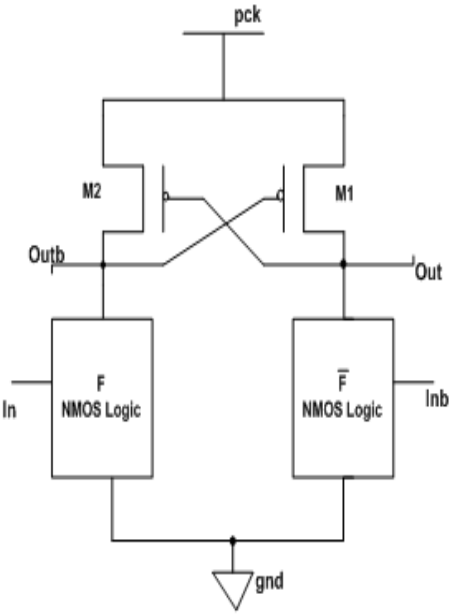

Fig.2. Efficient Charge Recovery Logic (ECRL).

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3. 2N-2N2P LOGIC

The 2N-2N2P is Inputs A and B will decide the output 'OUT' which will implement the true logic that is AND logic and output /OUT will implement the complemented logic that is NAND logic. When both or any one of A and B inputs are at logic low then the path connecting the power clock to Out will be open, while the other path connecting CLK to /OUT will be on. And thus, /OUT will follow the power clock in the evaluation phase and will be charged to logic high. This high logic will turn off the PMOS and turn on the NMOS connected to true input and thus output OUT will become logic low. Now, when both the inputs A and B are high, then the path connecting the output OUT to CLK will be turned on and thus output OUT will become high following the CLK. This high voltage at OUT node will turn off the PMOS and turn on the NMOS connected to inverted inputs and thus output /OUT will fall to logic low. [10, 17-19].

4. Positive Feedback Adiabatic Logic (Pfal)

The Positive Feedback Adiabatic Logic (PFAL) the implementation of different logic gates (AND/NAND, OR/NOR, XOR/XNOR respectively) using proposed ON OFF DCDB-PFAL logic. The evaluation of logic would be same as that for PFAL logic family without any difference. The functional blocks implementing different logic gates are connected to the pull up PMOS transistors through power clock 'CLK' [13, 20-22].

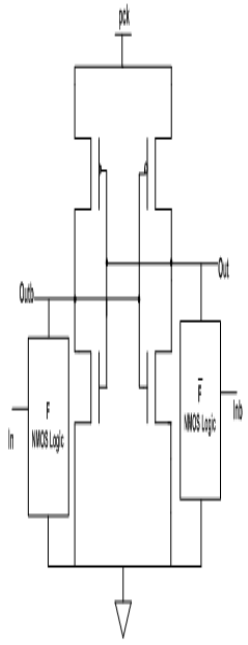

Fig.3. 2N-2N2P Basic Logic circuit.

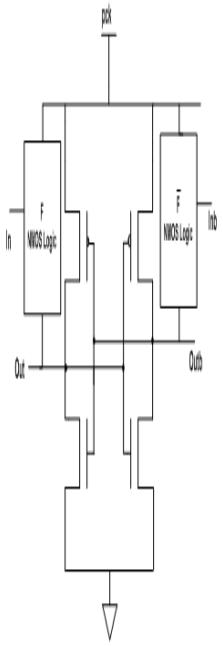

Fig.4. PFAL Basic logic circuit.

Assuming input IN High, the device MN3 in F logic block conducts and pulls the OUT node towards power clock CLK, which makes MP2 to switch off and /OUT is disconnected from power clock. This structure provides complete charge recovery by eliminating the charge stored in the output node after the recovery phase. Simulated result in Fig 5 (a) & (b) shown below [23].

We have implemented different logic gates, AND, OR, NAND, NOR, XOR, XNOR using the proposed ON OFF DCDB-PFAL adiabatic logic circuits. Same AC power supply trapezoidal clock is used in the realization of all these circuits. In order to avoid the use of inverters in an adiabatic logic circuit both inputs and outputs are dual rail encoded. Therefore both the positive and negative logic function is available using a single logic circuit.

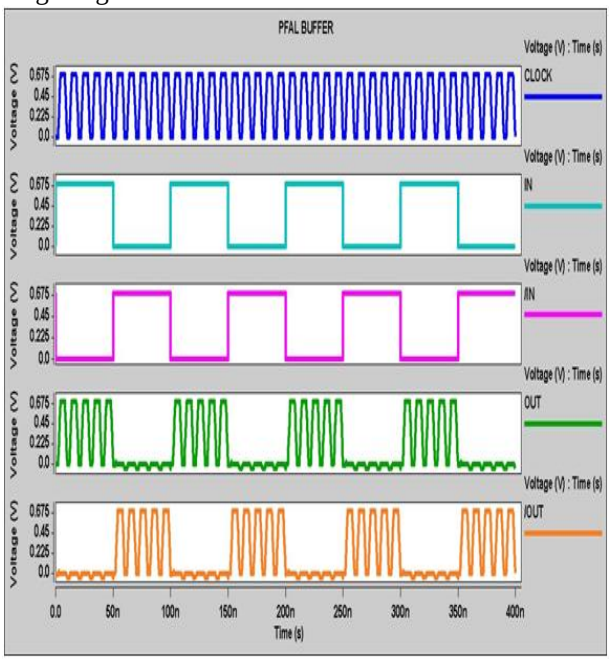

Fig. 5. (a) Basic Structure of Two input PFAL BUFFER Logic (b) Simulated waveform of PFAL BUFFER Logic.

III. SIMULATION AND RESULT

It can be seen from the readings of different tables and graphs plotted for different logic circuits at different frequencies that the proposed logic circuit has the lowest power dissipation among all logic circuits discussed in this paper. The DCDB-PFAL BUFFER has 90% less PDP as compared to PFAL BUFFER. Proposed NAND gate has 87 % less PDP as compared to PFAL NAND gate. Proposed NOR gate has 76 % less PDP as compared to PFAL NOR gate. XOR gate has 89 % less PDP as compared to PFAL XOR gate. Also by observing the readings from different tables, it can be said that delay remains less than all other circuits. That is, the proposed modified PFAL logic family provides much lower power dissipation without affecting the speed of operation of the logic circuit as compared to

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that of conventional PFAL adiabatic logic family and also over the other adiabatic logic circuits.

Table I: Design Parameters

TYPE	CMOS	Adiabatic Logics
PMOS (width)	260 nm	260 nm
NMOS (width)	130 nm	130 nm
Power supply	1 V DC supply voltage	Trapezoidal power clock, 0v- 1v ,frequency: 200MHz
		Rise Time: 1.25 ns, Fall Time: 1.25 ns

Table II: Average Power Dissipation for Different Logic Devices.

Logic	Gate	Power (Nw)	Delay (Ps)	Pdp (Zj)
2N2N2P	INVERTER	2.174	103.4	224.7
	NOR	2.049	107.6	220.4
	NAND	2.512	146.4	367.7
	XNOR	3.894	238.8	929.8
DCPAL	INVERTER	1.355	35.75	48.44
	NOR	1.45	37.35	54.15
	NAND	1.748	54.64	95.51
	XNOR	3.053	128.3	391.6
2N2P	INVERTER	1.164	35.98	41.88
	NOR	1.279	37.44	47.88
	NAND	1.579	54.92	86.71
	XNOR	2.747	144.6	397.2
PFAL	INVERTER	.3432	13.31	4.568
	NOR	.6828	9.398	6.417
	NAND	.6553	27.25	17.85
	XNOR	1.241	30.21	37.49
PROP CKT	INV	.281	12.57	3.532
	NOR	.5054	8.196	4.142
	NAND	.4551	27.13	12.34
	XNOR	.9634	30.17	29.06

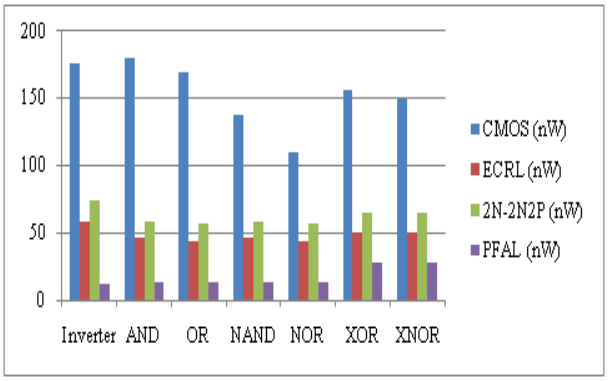

Fig.6. Comparison of Average Power Dissipation for Conventional CMOS and Different Adiabatic Families.

IV. CONCLUSION

This paper reviews the adiabatic logic circuits and the proposed circuit has been successfully designed and simulated by HSPICE tool at 32nm and 32nm technology at different frequencies of 10MHz, 500MHz, 1GHz. The main aim of this circuit is to reduce the power consumption of the circuit. In addition to the power dissipation, delay and then power delay product are also determined. The previous work is improvised by applying different technique. This method provides the easier way to reduce leakage current and hence, power consumption.

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