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Performance Analysis of SISO-OFDM Architecture for Wireless Applications using VLSI Technology

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***Abstract*-Novel technologies have started emerging as an evolution of wireless communication standards, and corresponding low cost devices are key to follow this trend in order to achieve better quality of service (QoS) and support large amount of users that can communicate simultaneously. Orthogonal Frequency Division Multiplexing (OFDM) is believed to be the key technology to meet all these demands. OFDM is a form of frequency division multiplexing with the special property that each tone is orthogonal to each other with every tone. OFDM has overcomes most of the problems with FDM and TDM. In many broadband communication technologies, OFDM modulation techniques are normally preferred. VLSI technology has now made progress in the region of small area and power. The proposed architecture is developed using Verilog HDL and implemented in altera cyclone IV E. The performance evaluation has been made in relation to latency, area and power.**

***Keywords*- Modulation, Orthogonal Frequency Division Multiplexing, Data rate, VLSI**

I. INTRODUCTION

For high speed data transmission, the mainly used standard is Orthogonal Frequency Division Multiplexing (OFDM) [7]. Orthogonal Frequency Division Multiplexing (OFDM) technology promises to be a key technique for achieving the high data rate and spectral efficiency requirements for wireless communication systems in the near future. OFDM has been adopted in many wireless standards such as worldwide interoperability for microwave access (WiMAX) and Long Term Evolution (LTE) [8]. Wireless communications techniques have been growing very rapidly in the last few decades.

Therefore more reliable wireless communication systems are required having higher spectral efficiency [8]. OFDM is a modulation technique or a multiplexing technique. OFDM can save fifty percent of bandwidth by dividing the available spectrum into many overlapping carriers. This multi carrier should be orthogonal. OFDM is a special case of multicarrier transmission, where a single data stream is transmitted over a number of low data rate subcarriers [7,8,9]. This low symbol rate will reduce theeffects of ISI. OFDM increase the robustness against frequency selective fading.

In single carrier system a single fade or interferer can cause the entire link to fail, but in multicarrier only a small percentage of the subcarriers will be affected OFDM also provides high immunity against multipath dispersion [10]. This paper investigates the model of OFDM architecture with its basic components. Performance results will be discussed over VLSI technology.The rest of the paper is organized as follows: Description of the transmitter and receiver model for OFDM system is given in Section 2. Components of OFDM discussed in Section 3. Performance results are shown in section 4 and paper is concluded in section 5.

II. DESIGN OF SYSTEM MODEL

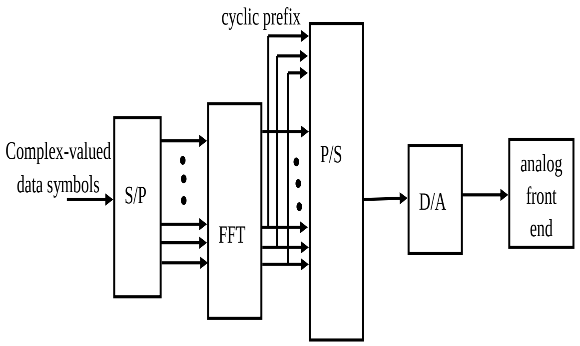

Fig. 1 Block diagram of an OFDM transmitter.

Fig. 1 shows the block diagram of an OFDM transmitter section. Serial data is fed to the block of OFDM as an input and the output is a 2-bit IQ. Therefore, the input sampler is a block with two bits in a group. The output of the input sampler is fed as input to the symbol mapper. The symbol mapper consists of an QPSK modulator which is divided into two 2-bit symbols called I and Q (Imaginary and Quadrature). These symbols are generated based on the constellation diagram. [5]The output from the symbol mapper is provided to the next block, Serial Input Parallel Output(SIPO). This block is used to convert the serial data into parallel data. SIPO is a two 8 register (0-7) array. The serial input is fed at the seventh array and for every clock cycle the data is shifted to the above register. After eight clock cycles the data in the array is forwarded. The SIPO output contains 8 registers for real and imaginary data. The Inverse Fast Fourier Transform (IFFT) input will the output from the SIPO. As required, the system consists of two IFFT modules, one for the real and the other for imaginary. The IFFT converts frequency domain to time domain. The time domain values are transmitted as OFDM signals through the transmitter.[5].

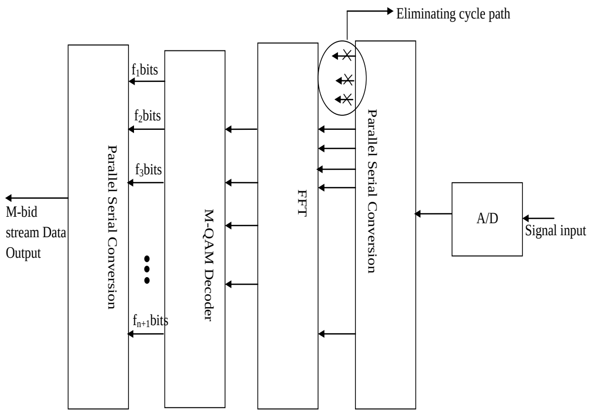

Fig. 2 OFDM receiver.

Figure 2 shows the OFDM receiver model. Serial input data is converted into word for transmission. Then Serial data is converted into parallel, assigning each data word to one carrier in the transmission. Demapper is used to convert complex valued constellation points to symbols. Each point consists of 2 bit data and resend to de-spreader block. The Process of demodulation is done by Fast Fourier Transform (FFT) which again converts the time domain into frequency domain signals.[5] This section concludes with basis of modulation and demodulation of OFDM signals.

III. COMPONENTS OF OFDM ARCHITECTURE

The major contribution of work has been done in the novel design of FFT, ENCODER and Interleaver in the OFDM architecture. Novel design of FFT using Booth Encoded Wallace Tree Multiplier is done which will reduce the Partial Product Generator (PPG) which in turn reduces the number of Logic Elements (LE) resulting in overall area consumption of 10% approximately.[19].Figure.3 represents a novel design of FFT architecture which consists of Butterfly units inside FFT unit, complex Booth Encoded Wallace Tree multipliers inset of Butterfly unit, Input buffer, Output buffer and the control unit. Real and imaginary data obtained after constellation is given to input buffer.

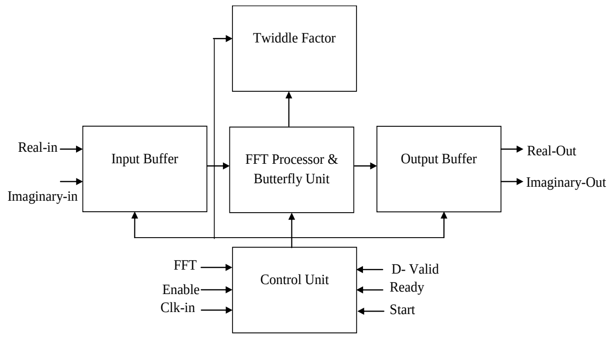

Fig. 3 Novel design of FFT with Booth Multiplier.

According to the input bit from input buffer, the real and imaginary values are passed to the butterfly unit for further computation of FFT logic. The butterfly units carry out complex addition and subtraction of two input data x[*n*] and x[*n* +*N*/2]. The output from each input signals in the butterfly units come from previous stage. Twiddle factor multiplication utilize multiplexers which are also present in the butterfly unit. The twiddle factor multiplication for FFT computation is accomplished by fixed-width complex multipliers. The complex multiplication requires a look-up table (LUT) using ROM to store the twiddle factor values [19].

Decoder is another important block in OFDM architecture. Max Log-Maximum APosterio Soft Input Soft Output (ML-MAP-SISO) decoder is another block in OFDM architecture. [13].Figure. 4 shows the proposed decoder which is used in OFDM architecture for our work. This Proposed decoder has overcome the numerical representation complexity, reduced the power consumption. In the receiver section, the received is converted into frequency domain using FFT initially and then cyclic prefix is removed. The proposed decoder is implemented in the de-interleave block of the OFDM and the data is passed through the signal demapper and Parallel to Serial converter to obtain the output. The inner block of De-Inter leaver was shown in Figure 5.

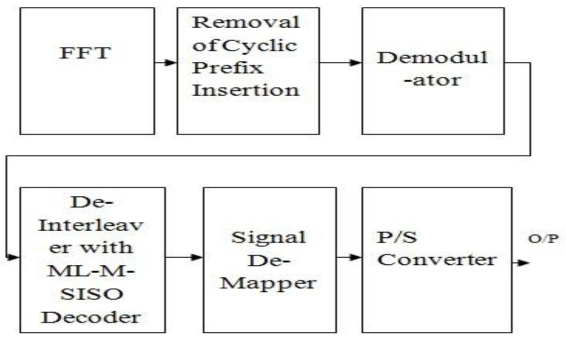

Fig. 4 OFDM Transmitter section with the ML-M-SISO Decoder.

The reverse process of the receiver is done in the transmitter side before being transmitted. Then the performance evaluation of the proposed system is computed in terms of chip area, Bit Error Rate and latency after implementation using VLSI technology. [20]

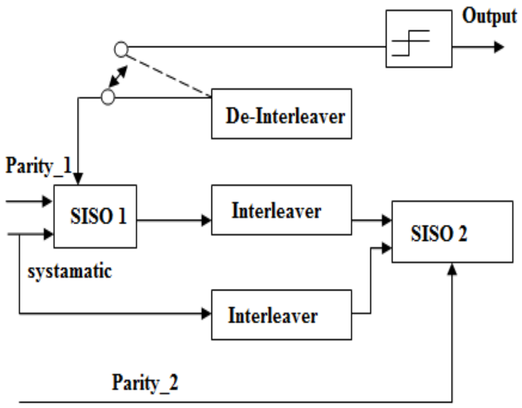

Fig. 5 The Inner Section of De-Interleaver.

In addition, to achieve maximum frequency, 2-step interleaver has been designed with the address generator based on Finite State Machine which supports OFDM.If the adjacent symbols are placed further than S, it results in the process of Semi-Random interleaver. For the specified states, the address tracking will be done by counter. Table 6.2 shows the inverted performance of the bit reversal operation and Look up entry for turbo Coder.[1].

Table 1 Look up entry for turbo Coder.

Table Index	n-5 Entries	n-6 Entries	n-8 Entries	n-9 Entries	n-10 Entries
0	3	15	3	13	1
1	27	127	1	335	349
2	15	80	5	87	303
3	13	1	83	15	721
4	20	31	19	15	973
5	5	15	170	1	703
6	1	61	19	333	781
7	31	47	90	11	327
8	3	127	23	13	453
9	9	17	1	1	95
10	15	119	3	121	241
11	31	15	13	155	187
12	17	57	13	1	497
13	5	123	3	175	900
14	30	95	17	421	769

Data from the adder and Finite State Machine (FSM) will be sent to the accumulator and fetch it to the processing block next to it as per the control signal, as shown in Figure 6. Based on the control statement, FSM will generate address for interleaver. These addresses are generated based on the preset logic and random access memory will act as storage element for the address generated by the finite state machine. Area efficiency will be the result for FSM based address generator implementation.

The top level design of interleaver is composed of address generator and interleaver memory. The memory block consists of two units namely RAM-1 and RAM-2, inverter and multiplexer. One memory block will be written to while the other will be read from and vice versa in block memory. The multiplexer with address input and select line sends the read and write address to memory module. First the write enable signal of RAM-2 will be active and so will receive the write address and RAM-1 will receive the read address. After the write process of RAM-2 is over the select line will change and the process is reversed. The interleaved data stream from the read memory block to the output is guided by the multiplexer present outside the memory block.[18].

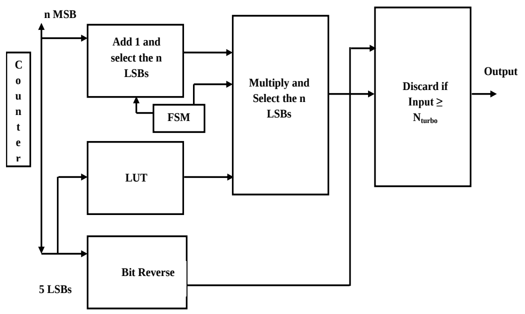

Fig. 6 Proposed Interleaver Architecture with FSM implementation.

This section concludes about the novel design of FFT, decoder and interleaver for OFDM architecture.

IV.PERFORMANCE ANALYSIS

The proposed architecture is simulated and synthesized using Verilog, with this entire feature of novel design of FFT, Interleaver and Decoder. [18,19,20]. Once the design is coded in VERILOG, the simulation and synthesis report is carried out by using 10.0c compiler and Altera Cyclone IVE.

Table 2 Synthesis Report for Proposed blocks in OFDM

Device elements	FFT	Decoder	Interleaver
Total logic elements	11739	695	23
Dedicated registers	8607	394	267
Memory bits	<1 %	<1 %	<1 %

Comparison results of proposed blocks of OFDM shows significant improvement in terms of power consumption and maximum frequency.

Table 3 Performance analysis in terms of Power, Area and Frequency

Performance Parameters	FFT	Decoder	Interleaver
Power	28 MW	37.84 mw	2.87mW
Area	$1.23mm^2$	$0.907\ mm^2$	$1.02\ mm^2$
Frequency	275MHz	120 MHz	193.53MHz

All the modules include FFT, Decoder and Interleaver have been created in HDL language and mapped to OFDM system. After correlation with the hard choice design the proposed framework provides better result as far as force and postpone. Along these lines, it presumes that the proposed framework can be utilized for Wireless application with huge region increment. Throughput obtained after integrating as a top module is 4.22 Gb/s.The maximum Frequency (Fmax) achieved is 267 MHz, and throughput achieved is 4.42 GB/s. Throughput is the measure of information that is prepared per clock cycle (bits per second), Latency is characterized as the time between information input and handled information yield (clock cycle). Throughput can be calculated by multiplying the number of bits and clock frequency. Therefore, Throughput= $16 * 267 * 10^6 = 4.4$ GB/s.

V.CONCLUSION

An advanced VLSI technology is required for OFDM which can be used in wireless applications. Basically OFDM is utilized for high transmission of data from Fading Channel. However, the important section in OFDM is FFT, which is quite complex to implement in real time hardware equipment, specifically in FPGA devices. Novel architecture of 512 point FFT using Booth encoded Multiplier, Decoder uses Soft Input and Soft Output algorithm for Max-Log Maximum a Posteriori (ML-MAP) decoder and Interleaver with address generation using Finite State Machine for 2-step interleaver is made. All the elements have been created in HDL language and mapped to OFDM system. Thus the proposed framework can be utilized for Wireless application with enormous growth.

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