

Techniques for Fully Integrated Intra/Inter Chip Optical Communication

Mrs. K.P. Joshi

Dept. of Electronic & Telecommunications
Dr. D.Y. Patil Polytechnic
Pune, India
kvtjoshi68@gmail.com

Abstract: - Inter/ Intra chip optical communication eliminates all data and control pads generally present in conventional chip. It replaces them with a new type of ultra-compact, low power optical interconnect communication technique. It enables entirely optical through-chip buses that could service hundreds of thinned stacked dies. Even in tight power budgets, very high throughputs and communication density could be achieved. The core of the optical interconnect is a CMOS single-photon avalanche diode (SPAD) operating in pulse position modulation. CMOS compatible optical interconnect techniques based on miniaturized optical channels. By using optical communication technique one can achieve high throughputs i. e. several gigabits per second at very low cost in terms of area and power dissipation, so as to represent a real alternative to conventional systems. In this seminar communication between inter/intra chip will be discussed using optical communication technique.

Keywords – Intra-chip & inter-chip communication, low power optical communication, miniaturized optical channel and detector.

I. INTRODUCTION

Evolution of IC technology causes system designs to move towards communication-based architectures. Metallic interconnect networks may be very costly in terms of power and silicon area hence become limitations in system on chip design. Integrated optical interconnect is becoming a potential solution to overcome predicted interconnect limitations identified by the International Technology Roadmap for Semiconductor.

In the technique like VLSI, it is becoming difficult for a copper based electrical interconnect to satisfy the multiple design requirements of power, bandwidth, delay and delay uncertainty, because electrical interconnects are becoming increasingly susceptible to parasitic resistance and capacitance. Multiprocessor systems on chip designs rely on these electrical interconnects at the physical level and are consequently faced with the challenges and drawbacks of it. Now a day's several research looking at interconnect alternatives such as on chip optical interconnects, carbon nano tube based interconnects and wireless interconnects

II. OPTICAL COMMUNICATION

Semiconductor industries face challenges in implementing high speed metal interconnects as silicon CMOS circuit technology is scaled above the GHz range. Performance of metal traces are limited in density-speed due to the electrical conductivity, skin

effect and cross talk, Optical based interconnects have much higher bandwidth more than 100 THz which is required for high carrier frequencies of optical signals.

1. Motivation to Optical Interconnection

To eliminate all data and control pads generally present in conventional chips and to replace them with a new type of ultra-compact, low power optical interconnect implemented almost entirely in CMOS. It makes optical through-chip buses can be used hundreds of thinned stacked dies. Even in tight power budgets very high throughputs and communication density could be achieved. The main component of the optical interconnect is a single-photon avalanche diode operating in pulse position modulation.

Now a new approach to optical communication is proposed that it can be integrated in standard CMOS technologies utilizing a fraction of the area and power of a pad. The core of the optical interconnect channel is a CMOS single-photon avalanche diode (SPAD). The device can detect very low photon fluxes, with minimum requirements of optical power at the source.

For low bit-rate intra-chip optical data communication a low-cost, high-density scalable technique is proposed. The data stream is modulated by a low-intensity photon flux. Then it is propagated through standard silicon layers. Single photon avalanche diode is used for photon detection and data demodulation.

III. OPTICAL TECHNOLOGY

Today, 0.18 micrometer CMOS technology enables a 3-GHz operational frequency for the Pentium 4 CPU. However poor wiring limits the data flow to only 533 MHz on the system bus. The overall performance of a computer is not limited by the speed of CPU, but by the ability to communicate rapidly between the CPU and other data processing units (memory and display chips). Although a copper connection can increase the connection speed, bit rates transmittable on electronic wires are fundamentally limited by the wire's parasitic resistance, capacitance, and inductance.

Connection speeds will never keep up with a CPU running at 10 GHz. Further, transmission speed drops dramatically with the propagation distance. Optical connections between circuit boards, electronic chips, and within one electronic chip are the ideal solution to remove this speed hurdle. Optical signals in free space or optical waveguides always travel at the speed of light independent of the size and the length of the optical wire (waveguide) and are free from electronic noise. For many high-end applications, an optical connection is the only connection technology that can keep up with the computation speed of the CPU. At present, optical connections between two computers are commercially available.

1. Optical Transmission of on-chip modulator

For optical transmission a laser source, a modulator, and a modulator driver (electrical) circuit is required. The laser source provides light signal to the modulator, which converts light signal into electrical information into a modulated optical signal.

Both off and on-chip laser sources are feasible. Off chip laser source has greater on area, chip power, and cost savings. As the light signal enters the chip, optical splitters and waveguides route it to the different modulators which are used for actual data transmission. These distribution paths are a source of signal losses. The modulator translates the electrical information from modulator driver into a modulated optical signal. High-speed electro-optic modulators are designed in such a way that the refractive index or the absorption coefficient of an optical path changes as the injection of an electrical signal changes.

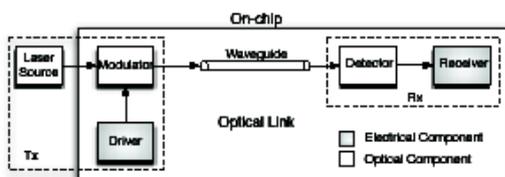


Fig.1 Simplified diagram showing the main components involved in on-chip optical transmission for transmitter and receiver

Recently optical resonator-based implementations are preferable among different types of proposed modulators for integrated circuit design, because of low operating voltage and compact size. Modulators are the optical equivalent of electrical switches and their performance is dependent up on the on-off light intensity ratio is called as extinction ratio; The Extinction Ratio is dependent upon the strength of the electrical input signal.

Transmission errors in the channel cause because of poor extinction ratio. Higher extinction ratio is better for proper signal detection. This ratio also puts limitations on the use of number of transmitters which can time-share the same wavelength on the same channel. Extinction ratio more than 10dB has been recently reported with high input signal swing.

Modulator size is another important criterion for integrated applications. There are so many significant recent activities related to compact-sized modulators. Already 10 μ m ring-modulators (circularly shaped) have been proposed, and their size is likely to be reduced with each successive generation, bounded by lithographic process and bending curvature limitations. The modulator driver consists of a series of inverter stages driving the modulator's capacitive load. A smaller capacitance will improve the power and latency specifications of the overall transmitter, thereby requiring fewer stages.

The core of the optical interconnect channel is a CMOS single-photon avalanche diode SPAD. This device can detect very low photon fluxes that ensure minimum requirements of optical power at the source. The detection cycle can be as high as a few tens of nanoseconds in single-photon avalanche diode. Thus, to achieve throughputs of several gigabit-per-seconds a simple digital modulation scheme must be added. Pulse position modulation (PPM) scheme encodes K bits into $2K$ time slots in the total allotted range R . To ensure proper operation of the communication link, R should be higher than the detection cycle.

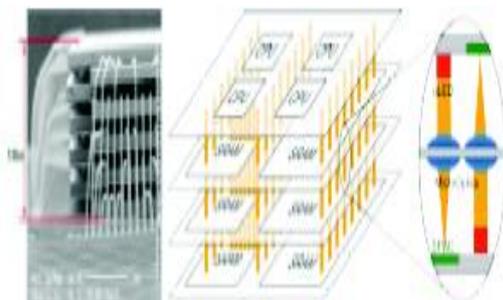


Fig.2 High density inter chip optical communication scheme.

Optical data signals are generated in an integrated CPU by a micro LED. A sub nanosecond optical pulse was recently used for this device using CMOS drivers. These drivers occupy a fraction of the area of a pad. The proposed optical interconnect architecture comprises a light source and an integrated driver and ultra-fast PPM coder/decoder logic. The PPM decoding process is obtained through a time-to-digital Converter. This component must distinguish the time-of arrival of one or more photons as detected by the SPAD.

2. Receiver

An optical receiver converts optical signal in to electrical signal. It consists of a photo detector and a trans-impedance amplifier stage. The detector section of the channel consists of single-photon avalanche diode and integrated PPM decoder. The optical channel using integrated micro-optics integrated on chip in most CMOS technologies. Multi-chip vertical buses can be obtained by stacking dies that have been thinned.

Optical transmission is ensured by low absorption coefficients of silicon in the visible spectrum. In wave division multiplexing (WDM) applications, different wavelengths are used for simultaneous transmission through waveguide. For each received wavelength the receiver requires a wave-selective filter. The photo detector that is most often proposed is a PIN diode. The photo detector's quantum efficiency is an important figure of merit for the system. High quantum efficiency means lower losses when converting optical information into electrical form. Detector size is also an important criterion for both compactness and next stage capacitance. Typically, the detector has large base capacitance and it became a design challenge for high-speed gain stages which are following to it.

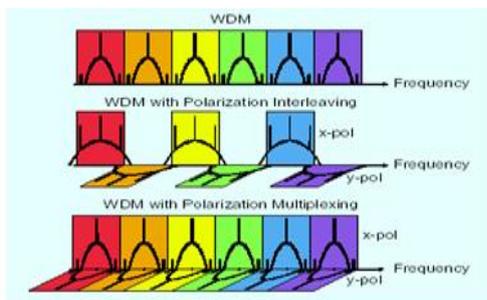


Fig. 4 Wavelength Division Multiplexing

3. Waveguide

Light is routed through waveguides. Refractive index of waveguide material plays very important role to decide bandwidth, latency, and area of the optical interconnect. For on-chip applications, silicon (Si) and polymer are the most applicable materials. Comparison of silicon and polymer waveguides on some of the most relevant features is given in Table 1. The smaller refractive index of polymer waveguides results in higher propagation

speed but it requires a larger pitch than Si, which reduces bandwidth density, the number of bits that can be transmitted per unit surface area

Table1 General Characteristic of silicon and polymer on chip waveguides.

Waveguide	Si	Polymer
Refractive Index	3.5	1.5
Width(μm)	0.5	5
Separation(μm)	5	20
Pitch (μm)	5.5	25
Loss(dB/cm)	1.3	1

4. Bus Design

In opto-electrical hierarchical bus, nodes deliver information to processors via electrical sublevels. A possible four-node organization for 64- processor is shown in fig.4. .In chip Multiprocessor CMP, every node is shared among four electrically interconnected L2 caches. Our bus comprises an address/command bus, a data bus, and a snoop response bus. Total 64 bits for address/command including ECC and tag bits, 72 bits to data including 8-bit ECC and assuming that tags are provided at the header, and 8 bits per snoop response are allocated. Therefore, the number of waveguides is 136 for address/command plus data buses, and 8n to support snoop responses.

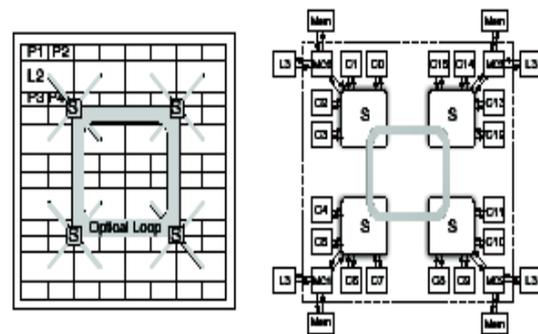


Fig. 3 Simplified CMP floor plan diagram (left) and high-level system organization (right), showing the optical loop and the rest of the hierarchical bus.

The proposed loop-shaped bus comprises optical waveguides (residing on a dedicated Si layer) that encircle a large portion of the chip. Multiple nodes connected to the bus, each of them responsible for issuing transactions on behalf of a processor or a set of processors, are equipped with necessary transmitters and receivers to interface with the optical medium.

Multi bus organization can be multiplexed by address and by node. While by multiplexing by address wavelengths are assigned to different address spaces. Any node can drive any of the w wavelengths so requires arbitration. Whereas multiplexing by node gives each of the n nodes exclusive access to w n

wavelengths. It has numerous advantages. But the number of nodes directly connected to the bus is then limited to wavelengths w . An important consideration for both organizations is to prevent the light from circulating around the loop for more than one complete cycle, or older messages can cause undesirable interference. Since the optical power in a continuous laser source based system is dependent upon the number of modulators.

IV. ELECTRICAL AND OPTICAL INTERCONNECTION

OI (optical Interconnection) possess an intrinsic advantage of low signal propagation delay in waveguides due to the absence of RLC impedances. Fig. 5 shows a comparison of signal propagation delay in copper based electrical interconnects (EI) and the two common waveguides silicon and polymer. Refractive index of polymer is low and for silicon wave guides is high. These are selected for the comparison, as are opposite types of optical waveguides in terms of signal propagation delay and crosstalk. Optical Interconnects provide a lower propagation delay than electrical interconnects.

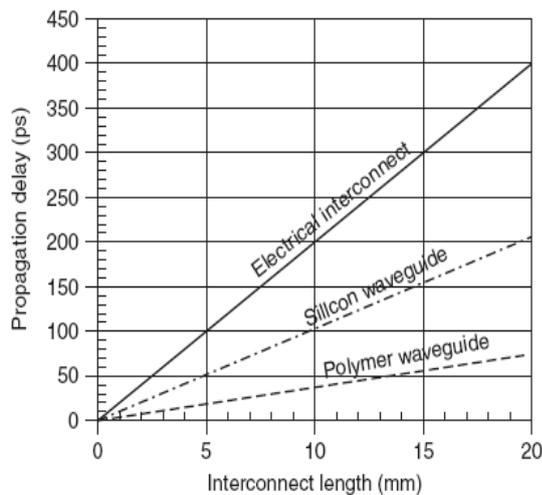


Fig. 5 Propagation delay of Si and Polymer waveguides compare to Electrical Interconnection.

This is because optical signal propagation is intrinsically faster than electrical signal propagation due to the absence of RLC impedances. It has been estimated that the combined transmitter and receiver delay should be lower than 280-370 ps for polymer waveguides and 180-270 ps for silicon waveguides, to have an advantage over Electrical Interconnections. The total power consumption for optical Interconnection should be less than 17-18 mW to have an advantage over EI power consumption.

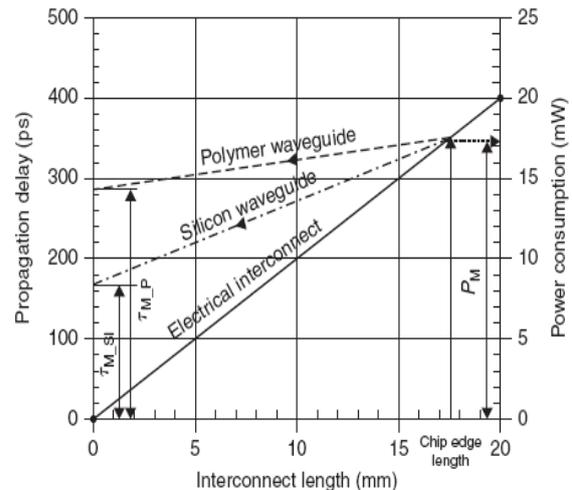


Fig.6 Propagation delay, power of Si and Polymer waveguides compare to electrical Interconnection.

1. Optical Interconnection (OI) Challenges

1.1 Efficient Transmitter and Receiver component:

It is required that high speed, low power and small feature size electro-optical modulators and photo detector receivers need to be developed. It should have combined delay and power dissipation which is lower than threshold required to be advantageous over EIs. Recently Mach-Zehnder electro-optic modulators with an ultra compact length of 100-200 μ m having low power consumption and high modulation efficiency were presented.

1.2 Integrated on-chip light source: The number of materials and processes available for optic inter connect fabrication is limited to these technologies that are compatible with micro electronics. Currently these limitations results in the absence of a monolithic on-chip light source. Innovative solutions such as Indium Phosphide hybrid silicon laser from Intel may solve this problem in future.

3. Temperature Management

On chip optical inter connect modules are very sensitive to temperature variations. Designers need to ensure that operating temperature for components are maintained or designed new optical inter connections structures that are not so sensitive to temperature. Either an active or passive optical control method will be required to maintain stable device operation.

V. APPLICATIONS OF OPTICAL INTERCONNECTION

1. R&D of element technique for future supercomputer

Research Objectives is apparently shifting to short range, intra equipment communication used in such systems as the next generation super computer and ultra high capacity routers. Japan is planning to launch a

project to construct a supercomputer by using this technology.

2. Application of optical Interconnection to inter node network

Kyushu University and Fujitsu Ltd. Are planning to develop Inter node optical Interconnection aiming at eliminating the inter node transmission bottleneck.

3. Application optical Interconnection to the CPU-memory link

Progress in the data transmission rate between the CPU and memory has been relatively slow compared with the amazing speed at which CPU performance has improved. This may be a worrying situation in future computers as the CPU-memory transmission rate limits the total performance of the system. NEC Corporation and Tokyo Institute of Technology are currently undertaking research into optical interconnection between the CPU and memory as an alternative technology for speeding up the CPU-memory.

4. Technology inside the chip: for a higher transmission rate

As the processing capacity continues to increase, the need for an optical link moves from the inter-node to inter-chip and further into the intra-chip level. NEC announced in February 2005 the successful development of a silicon photodiode that can be used as an optical receiver for intra chip optical link.

VI. CONCLUSION

Optical communication is used to eliminate all data and control pads generally present in conventional chips. So Optical Communication provides a real alternative to conventional recent techniques because of high throughputs at very low cost in terms of area and power dissipation. Optical Interconnects provide a lower propagation delay than electrical interconnects. Optical signal propagation is intrinsically faster than electrical signal propagation due to the absence of RLC impedances. The total power consumption for optical Interconnection should be less than 17-18mw to have an advantage over EI power consumption. The optical communication within two computer boards (inter-board) will be available in 2-5 years; a chip-to-chip communication (inter-chip) will come onto the market within 5-10 years, while an on-chip optical connection within a VLSI electronic chip (intra-chip) might become available in two decades.

REFERENCES

- [1]. N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, "Analysis and Design of Inductive Coupling and Transceiver Circuit for Inductive Inter-chip Wireless Super connect", IEEE J. of Solid-State Circuits, Vol. 40, N. 4, pp. 829 - 837, 2005.
- [2]. C. Niclass and E. Charbon, "A CMOS Single Photon Detector Array with 64x64 Resolution and Millimetric Depth Accuracy for 3D Imaging", IEEE Intl. Solid-State Circuit Conference (ISSCC), pp. 364-365, Feb. 2005.
- [3]. J. Song, Qi An, and S. Liu, "High-Resolution Time-to-Digital Converter Implemented in Field-Programmable-Gate-Arrays", IEEE Trans.on Nuclear Science, Vol. 53, N-1, 2006.
- [4]. C. A. Barrios, V. R. de Almeida, and M. Lipson. "Low-power consumption short-length and high-modulation-depth silicon electrooptic modulator". Journal of Lightwave Technology, 21(4):1089-1098, April 2003.
- [5]. C. Niclass and E. Charbon, "A CMOS Single Photon Detector Array with 64x64 Resolution and Millimetric Depth Accuracy for 3D Imaging", IEEE Intl. Solid-State Circuit Conference (ISSCC), pp. 364-365, Feb. 2005.
- [6]. V.R.Almeida,C.A. Barrios, R.R. Panepucci, M. Lipson, M.A. Foster, D.G. Ouzounov, and A.L. Gaeta. " All-optical switching on a silicon chip". Optics Letters, 29 (24) :2867, December 2004.
- [7]. M. A. Blake, S. M. German, P. Mak, A. E. Seigler, and G. A. Huben. "Bus protocol for a switchless distributed shared memory computer system". United States Patent#6,988,173 B2, International Business Machines Corporation, January 2006.
- [8]. G. Chen, H. Chen, M. Haurylau, N. Nelson, P. M. Fauchet, E.G. Friedman, and D. Albonesi. Predictions of CMOS compatible on-chip optical interconnect. In International Workshop on System-Level Interconnect Prediction, pages 13-20, San Francisco, CA, April 2005.