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A Review Article of Instrumental Amplifier 16 Bit Pipelining ADC

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Abstract **– Analog to digital converter is the important component in signal processing and communication system. It is a mixed system which converts the analog signals into the digital signals for transformation of sensor data. There are many types of ADC's available such as pipeline ADC, successive approximation ADC, delta sigma ADC etc. In present day CMOS technology the flash ADC is composed by utilizing the dynamic method, it reduces the power, and delay. A flash ADC is extremely valuable for fastest speed operations when it is compared with the other ADC architectures. Comparator and Encoder are vital part of flash ADC. This paper presents review of Efficient Low Power High Speed Flash ADC Techniques.**

Keywords**—ADC, Flash ADC, Resolution, Conversion rate, Comparator, Conversion speed, Encoder.**

I. INTRODUCTION

The increasing number of communications protocols and the expanding world of digital communications call for companies to produce more versatile devices. Devices such as cellular telephones and software radios are often designed to operate using more than one method of reception to increase the number of locations in which the device may be used. At the time of this writing most cellular telephones can receive both analog and digital signals. Implementing a number of different receiver types in one device can be very expensive. There is definite need for easily implemented designs that accommodate several different communication protocols in a single device. Many newer receiver architectures call for the signal to be digitized as early as possible. The remainder of the processing is left to lower power, reliable digital circuits more cheaply realized than their analog counterparts. In order for this to happen, the analog-to-digital converter (ADC) systems that quantize the incoming signals must become versatile and easy to implement. Sigma-delta (CA) ADCs provide a high degree of resolution using low complexity components at a high sampling rate. The biggest drawback to using these quantizes is that the increased resolution is achieved in a very narrow band of frequencies compared to the sample rate. However, the insensitivity to circuit matching makes this converter a good candidate for multiband conversion. The outputs from multiple quantizes run in parallel can be combined to achieve the high resolution of the CA ADC over a much wider bandwidth [1-2].

II. RELATED WORK

An increasing number of IC compatible sensors demand suitable readout circuits with on-chip ADC to reduce the signal sensitivity to perturbations on the circuit and at the sensor interface, decrease system complexity and cost, as well as enable further on-chip digital processing like data correction. Applications like wireless sensor nodes and medical diagnose always require at least 12-bit linearity and noise performance and extremely low power consumption (as low as 100µW) because of the battery operation. In addition, to meet the requirements of large sensor arrays, the ADC must occupy small silicon area and can be multiplexed between multiple channels. A 100 µW, 13bit ADC used for sensor array applications is presented in paper [3]. The ADC employs an extended counting architecture in which the residual error from a first-order incremental modulator is encoded by a cyclic ADC to achieve high accuracy at a relatively high speed. Hardware reuse technique is utilized for low power consumption and small silicon area. The prototype ADC is implemented in 0.18 µm CMOS technology with 1.8V supply voltage and the core area is only 0.06mm2 including control logic. The ADC shows a peak SNDR/SFDR of 65.4dB/71.9dB.

This paper gives survey on various techniques of Flash ADC design. Researchers have implemented flash ADC with different number of bits and different CMOS technologies. Steven B. Kaplan et.al [1] proposed a complete transient digitizer system consisting of a superconductive flash ADC, on chip acquisition hardware, a room temperature interface and HYPRESS to digitally reconstruct the input signal. Transient digitizer with a near term performance of at least 6 effective bits at 10 GHz and 8 effective bits at 2.5GHz are obtained. The wide bandwidth of the digitizer front end has been demonstrated in beat-frequency tests up to 30 GHz. Yun-Ti Wang et.al. [2] Proposed an 8-Bit 150-MHz CMOS ADC with 0.6µm CMOS technology with 8 bits Resolution. An 8- bit 150-MHz CMOS ADC has been described that incorporates sliding interpolation, distributed sampling, interleaving, clock edge reassignment, and punctured interpolation. Siamak Mortezapour et.al. [3] Proposed a 1-V, 8-Bit

Successive Approximation ADC. The ADC consumes less than 0.34mW and has an ENOB of 7.9 for a 1-kHz input with close to rail-to-rail signal swing. This design demonstrates that low-voltage ADC with medium accuracy can be realized without requiring special enhancements to CMOS technology.

Table 2.1 Related work.

Author	Architecture	Resolution	Input voltage	Technology	Improved Parameters
Mamta Gurjar et.al [15]	3 bit flash ADC	3 bit	0 V to 0.7 V	45 nm COMS	Speed-5.3 Gs/s Bandwidth-16.65 MHz
Mingzhen Wang et.al [7]	4 bit flash ADC	4 bit	1.2 V	130 nm CMOS	Power consumption- 1.35 m Conversion rate- 2.5GHz
Pradeep Kumar et.al [12]	3 bit flash ADC	3 bit	1.3 V	0.18um CMOS	Power consumption- 36.273mw
Parthasarathy K. P. et.al [21]	6 bit flash ADC	6 bit	0.8 V	90nm CMOS	Power dissipation- 7.67mW.
Gulrej Ahmed et.al [20]	6 bit flash ADC	6 bit	1.2 V	65nm CMOS	Speed-1 GHz
Conor Donovan et.al [4]	6 bit flash ADC	6 bit	2.2 V	0.25um CMOS	Power dissipation- 150 mW
Prof. S.S. Khot et.al [9]	4 bit flash ADC	4 bit	0.7V	45nm CMOS	Power consumption- 145µW
Panchal S. D. et.al [13]	4 bit flash ADC	4 bit	2.5 V	0.18um CMOS	Gain- 72.5 dB at 150Hz 14.1 dB at 100MHz Bandwidth-2.511E6 Hz
S. S. Khot [23]	6 bit flash ADC	6 bit	2.5 V and 3.3 V	0.25 µm CMOS	Speed- 500- 565msps
Sunghyun Park et.al [6]	4 bit flash ADC	4 bit	1.8 V	0.18 µm CMOS	Power consumption- 78 mW

Conor Donovan et.al. [4] Proposed a 6-bit prototype converter built in a standard 0.25µm digital CMOS process which dissipates 150mW from a 2.2-V supply at 400 MS/s. It occupies 1.2 mm^2 and describe a digital technique that can removes the accuracy constraints from the comparators. Christophe Sandner et.al. [5] Proposed a 6 bit flash ADC, large analog bandwidth and low power in 0.13 µm CMOS copper technology with 1.2GSps. This ADC attains to an effective resolution bandwidth (ERBW) of 700 MHz when working at 1.2 GSps requires 160mW power and at 600 MSps accomplishes an ERBW of 600MHz with just 90mW power consumption from 1.5V supply. The chip area is 0.12mm2 and requirement for reference resistor step, implicit sample and hold operation, no edge impacts in the interpolation network when contrasted with resistive addition and input capacitance is low of just 400fF and because of that safely drivable analog converter can be interface. This configuration demonstrates the efficiency of the capacitive interpolation construction modeling with distributed sample and hold for flash ADC in GHz range. Sunghyun Park et.al. [6] Proposed 4-GS/s 4-bit Flash ADC in 0.18-um CMOS. It achieves a measured DNL and INL of less than one quarter LSB at 4 GS/s. The measured ENOB is 3.89 bits at 4 GS/s with a 10 MHz input, and 3.47 bits at 3.4 GS/s with an 800 MHz input. Mingzhen Wang et.al. [7] Proposed a 4 bit flash ADC with high spurious free dynamic for high data transmission correspondences using 130nm CMOS technology. They proposed timed digital comparator with dynamic offset concealment to enhance the ADC dynamic performance. This flash ADC has two and half clock cycle latency. It has low input capacitance of 300fF. The power consumption is 1.35mW with 1.2V supply. It has 2.5GHz conversion rate using a multi-stage pipelined design. This flash ADC enhances high sampling rate, low power, and low input capacitance and there is no need of any reference resistor stage.

III. SIGMA DELTA ADCS USED FOR CHANNEL QUANTIZERS

Sigma delta ADCs are able to quantize signals with a high degree of resolution, provided the signal energy is located at low frequencies compared to the sample rate. Using an integrating feedback loop, this converter applies a delay to the signal input and a noise shaping transfer function to the quantization noise. Signals that reside outside the narrow baseband region that is quantized with high resolution are pushed into the quantization noise that is shaped away from baseband. Using a one-bit quantizer and a one-bit digital-to-analog converter (DAC), Sigma delta ADCs are capable of achieving greater than 16-bits of resolution [8].

The Sigma delta ADC has been previously employed in a multiband scheme that used one low pass converter and several band pass devices [9]. A high degree of resolution was achieved across a bandwidth quantized by four devices. This work supports the idea that the Sigma delta ADC is a strong candidate for the quantize used in each channel of the proposed structure due to the high resolution achieved by the converter. It is well suited to Very Large Scale Integration (VLSI) technology as it uses circuits that do not have to be well matched to produce high precision outputs.

IV. PURPOSE OF THE RESEARCH

The purpose of this research is to formulate architecture that makes use of identical quantizes operating in parallel to efficiently perform wideband conversion. Each channel in the architecture contains identical hardware, so the cost of additional bandwidth is additional channels. The

desired result is a structure that is able to recombine a number of smaller bandwidth signals into one with larger bandwidth. The recombined signal should have as little magnitude and phase distortion as possible across the total recombined bandwidth, including where the edges of the smaller bands meet. The main focus of this thesis is the digital processing that allows the resolution of these parallel devices to be reliably extended to cover the first Nyquist band, which is half of the sample rate.

V. QUANTIZATION

Quantization is also necessary for analog-to-digital converters. Quantization is the process of assigning certain ranges of values from a continuous signal range to discrete values. This assignment creates quantization errors. A quantization error is the difference between the quantized value and the original signal. In Figure 1, the original signal vin is shown in blue. If a sample of this signal is taken at time T1, it would be quantized to n2, as shown in Figure 1. The difference between the sample of v_{in} and its quantized value n2 is indicated by the black bar.

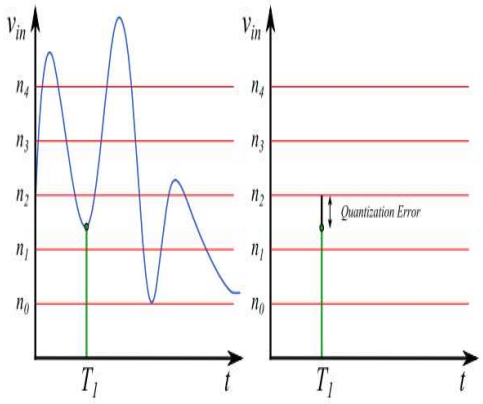

Fig. 1: Quantization errors of ADCs.

Quantization errors are directly related to the resolution of the ADC. An ADC that needs accuracy within a very small margin of error is going to need more quantization levels. More levels require a larger number of digital bits to encode all the information. Higher resolution often comes at the cost of converter speed, so converters need to be optimized for required speeds and resolutions. This optimization depends greatly on the type of architecture chosen for the ADC design.

VI. CLASSIFICATION OF ADES

Analog-to-digital converters are often divided into three major categories based on converter speed and accuracy. Table 2 was adapted from [10].

Low Speed, High Accuracy Some converters that are characterized by low speed and high accuracy include the integrating ADC and the sigma-delta oversampling ADC. Integrating converters are slow and their conversion times are proportional to the input voltage. Integrating ADCs require, in general, 2N clock cycles for N bits of resolution. A higher resolution means a slower conversion time [8]. Moderate Speed, Moderate Accuracy Other converters can be categorized by moderate speed and moderate accuracy. Successive approximation register ADCs and cyclic ADCs are both included in this classification of converters. [8]

Table 2: Classification of ADCs

Low Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low Accuracy
Integrating	Successive Approximation	Flash
Oversampling	Algorithmic	Two-Step
		Pipeline
		Time-Interleaved

A selection of ADC architecture types with their respective sampling rate and resolution ranges can be seen

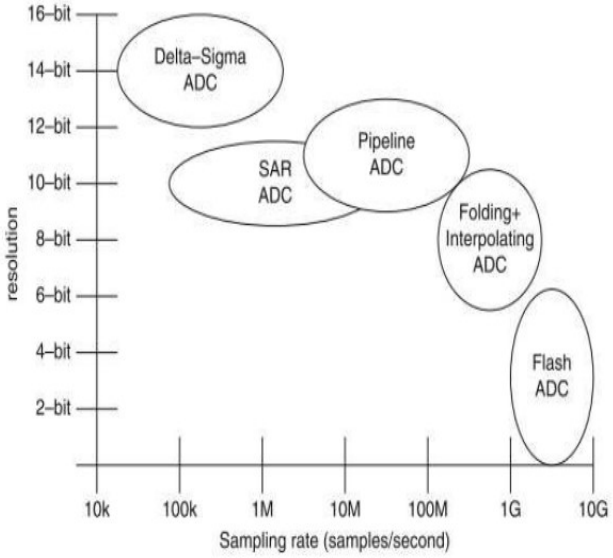

Fig. 2: ADC Architecture Comparison [1].

VII. SAR ADC

The SAR architecture algorithm is often described as being similar to a binary search algorithm. One common analogy for a binary search is looking for specific information on a page of a book. The searcher does not

know the correct page and can only ask the book's owner "yes or no" questions. The search would begin by starting at the center of the book and asking if the page being searched for is a higher number than the current page. If it is, then divide the upper half of the book in half and ask the same question for the new halves until there is only one page left. The decisions algorithm for a SAR converter is shown in Figure 2. The SAR ADC follows a similar algorithm that compares input voltages and reference voltages to determine a digital output value. The main advantage that a SAR design offers is the use of only a few analog components, particularly the use of only one comparator that results in a compact area and simpler design. The trade-off for this space is made in the maximum sampling rate. A converter with a sampling rate fs would require the comparator, DAC and SAR logic, shown in Figure 2, to operate at Nfs.
Advantages: The main advantage of SAR ADC is good ratio of speed to power. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. This SAR ADC will be useful for high speed with medium resolution and low power consumption.

VIII. CONCLUSIONS

This thesis has presented the design, layout, and test of a successive approximation register analog-to-digital converter. The background of the SAR converter, as well as general characterization of ADCs. The methods and decision processes for designing the analog portion of a SAR converter. Namely it talked about the design of the capacitive DAC, comparator, and biasing circuitry. The layout techniques used for each part of the converter, and what was necessary to put these devices into actual silicon. The necessary steps for testing and evaluating the newly fabricated converter. The ultimate goal of the converter was to have the split ADC correction algorithm applied to it. The novel idea needed to implement this algorithm was the individual selection of unit capacitors to make up different bits within a conversion. Because of this, existing SAR converters could not be used to implement the algorithm. A new successive approximation converter thus needed to be designed and implemented. The work presented here implemented a new SAR integrated circuit in the Jazz 0.18µm CMOS process. The new converter was then tested, the output data collected, and the correction algorithm was applied off chip to demonstrate the concept. [5]

FUTURE WORK: If research is to move forward with the split SAR concept, a better performing converter would need to be designed. The design mistakes in this work would need to be fixed. Namely the preamplifier oscillations would need to be remedied, and the input sampling nonlinearity would need to be eliminated. These two problems greatly degraded the overall performance of this converter. With the degraded performance, it was difficult to determine how much of an improvement the split ADC algorithm is capable of making. With the given hardware, the algorithm was able to make some improvement in the linearity of the output codes. However, that improvement was limited by the poor performance of the converter. To get a better idea of the impact of the correction algorithm on a SAR converter, a new converter would need to be fabricated. Special attention must be paid in simulation to the preamplifier and sampling circuit designs.

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