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Analysis of Performance Metric of Finfet Based SRAM Cell

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***Abstract* - For molecules to be used as components in molecular machines, methods that couple individual molecules to external energy sources and that selectively excite motion in a given direction are required. Significant progress has been made in the construction of molecular motors powered by light and by chemical reactions, but electrically driven motors have not yet been built, despite several theoretical proposals for such motors. Here we report that a butyl methyl supplied molecule adsorbed on a copper surface can be operated as a single-molecule electric motor. Electrons from a scanning tunneling microscope are used to drive the directional motion of the molecule in a two-terminal setup. Moreover, the temperature and electron flux can be adjusted to allow each rotational event to be monitored at the molecular scale in real time. The direction and rate of the rotation are related to the chiralities of both the molecule and the tip of the microscope (which serves as the electrode), illustrating the importance of the symmetry of the metal contacts in atomic-scale electrical devices.**

***Keywords* – FinFET, SRAM Cell, SNM, Read Delay etc.**

I. INTRODUCTION

The past 4-5 decades cmos scaling from one technology hard growth to the next net-work point has given got well operation. This made able to in getting greater, stronger, more complete smaller, quicker and powerful by numbers, electronic systems. But scaling of the greater size cmos is facing a great amount of questions because of, in relation to material and process technology limits [1].

As per 2011 International Technology roadmap for semiconductors 1 (ITRS) there are many questions to be made house numbers to the increased scaling of the greater size cmos cover Short Channel effects (Sces 2), such as sub-threshold loss, Drain got wall to keep others out lowering dibl and gate-dielectric loss and so on. The system level of being ready for working and system operation are acted-on because of, in relation to questions of cmos scaling.

Many persons making observations and men of science are working on cmos scaling and first one, then the other material ideas of semiconductors 1 to over-come the above said questions and attempting to put ball in play all the purposes of electronics and knowledge processing machine time. We have new apparatuses called FinFETs which are double-gate field-effect transistors 3 and are able of over-coming the scaling obstacles [1,2]. one of the most important features of FinFETs is that the front and back Gates helps in working well controlling the lightest electric part of all material move liquid-like through the narrow way for this reason get changed to other form the short narrow way effects [3-4].FinFET technology is strong person going up for position for future 10e-09 electronics because of, in relation to its high-performance 4, low power using up, made lower, less sensitivity to process different in some way, and take in of making using current processes.

The doing a play of SRAM system-part is strong of purpose primarily by the loss (waste) of time had to do with in driving greatly sized amounts on the bit line and the word line. Because of, in relation to the complex size of the on bit broken out SRAMs in small computers designed in nanometer nodes, leakage current is the major contributor to the total power dissipation in SRAMs. The exponential increase in leakage current results in large standby power.

Increased transistor leakage and parameter variation present challenges for scaling of conventional six-transistor (6-T) SRAM cells [5, 6]. The SRAM array parametric standby leakage contributors include well isolation leakage [7, 8], subthreshold device leakage [9] and gate-oxide tunneling current [10, 11]. The

major concern in future SRAMs is the leakage power consumption. Due to the reduced threshold voltage in future technologies, leakage power is increasing rapidly. Different SRAM cell designs have been proposed to target leakage control [12–13] finfet based SRAMs power against danger to un match got by process different in some way becomes quite necessary. Although there are some reports on the force of meeting blow of parameter 1 fluctuations 2 in Fin FETs by straight to measurement [14, 15], the sensitivity of finfet SRAMs without change, unmoving to process different in some way and methods to give greater value to such without change, unmoving have not yet been regularly made house numbers to the best of our knowledge.

A finfet uses a part within of body. It greatly keeps secret the device-performance changing one way and then the other caused by the fluctuation 3 in the number of dopant ions 4, while a planar-bulk mosfet has need of a heavily doped narrow way which causes serious process changing one way and then the other. It is able to be put before to stretch the 6-transistor SRAM power by effectively takeng advantage of the FinFET-based technology together with the new way taken by electric current way of doing. increased process different in some way in short narrow way transistors 5 is making feeble, poor the being strong of size fin 6 based SRAM.

Finfet based SRAM design has been offered as a that possibly taking place in addition answer to the size apparatuses. This also results in made lower, less without change, unmoving of SRAM prison room. finfet is right for future nano scale 7 memory journeys round design because of, in relation to its made lower, less Short Channel effects (SCE) and loss current.

In this book division, the observations of at rest Noise amount in addition (SNM), read Noise amount in addition rnm write Noise amount in addition (WNM) and noise in back power with different in some way of distance from side to side of way in, amount and person driving transistor 8 have been doed for the without change, unmoving of finfet based SRAM unit. HSPICE simulation 9 results have been presented for the SNM, rnm and WNM.

1. FinFET

The finfet based transistors 1 offers good trade-off for power as well offering interesting delay. Fig 1 shows a simple structure of finfet it is a 4 apparatus at end of system apparatus has among its parts of starting point and drain connected by a narrow way, the narrow way is covered up around by number times another Gates, in this Case we take into account 2 Gates namely forward and slow in development Gates or front and back Gates. A finfet is like a fet but the narrow way has been turned on its edge and made to be positioned up for this reason structure gave the name for the apparatus as finfet. FinFETs may be used for another into a former bulk-CMOS design by merely shorting the front- and back-gates together during apparatus making to let only one number making payment to see play connection per finfet This transistor 2 form is often telephoned shorted number making payment to see play (SG).The apparatus parameters 3 points to be taken into account are one of the important steps in getting greater, stronger, more complete a food to give strong taste design to be copied and then acting the part of it. commonly used finfet simulation 4 models ready (to be used) to the operation of making observations town are the quality to do with stating before-hand the future of Technology design to be copied (PTM)[14] and BSIM-CMG/BSIM-IMG[15].

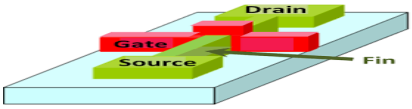

Fig.1 Fin FET.

2.SRAM Cell

The noise in back random-access memories (SRAM) are most widely used, because of, in relation to their high operation: small computers may have within up to 70% of SRAMs in transistor 1 count 2 or area[2]. The general direction in the semiconductor 3 market is to push for more joined as complete unit and more size copies of smaller size: the development and making the most out of a technology-based net-work point is more and more hard and high in price.

The being made less in size of a SRAM way taken by electric current in coming net-work points is all the same complex and it faces several limiting conditions. The level of being ready for working of the SRAM bit-cell is gave lower, less important position with ever smaller technologies and the apparatus workings is put in danger. designing SRAM journeys round in cmos 45nm has need of special to some science or trade and technology-based answers to over-come the size being made less limiting conditions, while giving insurance pleasure able workings, with a gave support to (a statement) level of being ready for working so that it can be by money and goods made.

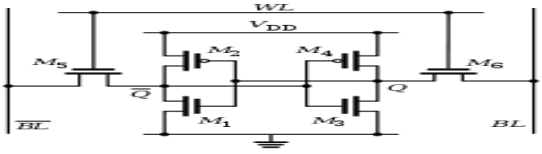

Fig. 2 6T SRAM Cell.

3. FinFET Based SRAM Cell

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The data storage cell, i.e., the 1-bit memory cell in static RAM arrays, invariably consists of a simple latch circuit with two stable operating points (states). Depending on the preserved state of the two-inverter latch circuit, the data being held in the memory cell will be interpreted either as a logic "0" or as a logic "1" .To access (read and write) the data contained in the memory cell via the bit line, we need at least one switch, which is controlled by the corresponding word line, i.e., the row address selection signal usually, two complementary access switches consisting of n MOS pass transistors are implemented to connect the 1-bit SRAM cell to the complementary bit lines (columns) [16-17]. This can be likened to turning the car steering wheel with both left and right hands in complementary directions.

The circuit structure of the full Fin FET static RAM cell is shown in Figure 3, along with the p FET column pull-up transistors on the complementary bit lines. The most important advantage of this circuit topology is that the static power dissipation is even smaller; essentially, it is limited by the leakage current of the pFET transistors. A FinFET memory cell thus draws current from the power supply only during a switching transition. The low standby power consumption has certainly been a driving force for the increasing prominence of FinFET SRAMs.

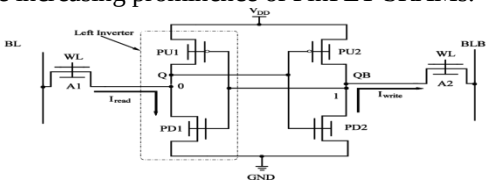

Fig. 3 FinFET Based SRAM Cell.

II. PERFORMANCE METRIC OF FINFET BASED SRAM CELL

1. Static Noise Margin

Stability, the immunity of the cell to flip during a read operation, is characterized by Static Noise Margin (SNM). SNM is calculated by the side of the largest square inside the FinFET based SRAM cross-coupled inverter characteristic measured during the read condition (BL 5 BL' 5 VD, and WL 5 VD) [18]. Static Noise Margin is the standard metric to measure the stability in SRAM bitcells. The SNM depends on the choice of the Vth for the FinFET's used in the SRAM cells. A high Vth means that drive current of these devices is small making the write operation more difficult, thus, increasing the SNM.

One approach to achieve a low power cell with high stability is to use high Vth devices at the cost of performance. FinFETs provide a high drive current even with larger Vth, thereby, achieving high noise margins along with good write stability [19]. The SNM is seen to be the most sensitive to threshold voltage fluctuations in the access and pull-down nFinFETs and least sensitive to the fluctuations in the pull-up pFinFET device. For FinFETs, the effect of Lg variation on Vth is small, so the effect on the SNM is also small.

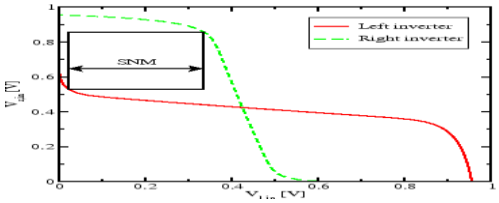

Fig. 4 SNM of 6T SRAM Cell.

2. Read Noise Margin

RNM is often used as the measure of the robustness of an SRAM cell against flipping during read operation [20]. For read stability (High RNM) of FinFET based SRAM cell, pull down FinFET is typically stronger than access FinFET. The read margin can be increased by upsizing the pull-down transistor i.e nFinFET, which results in an area penalty and/or increasing the gate length of the access FinFET increasing the 'WL' delay and hurting the write margin.

A careful sizing of the Fin-FET device is required to avoid accidentally writing a 1 into the cell while trying to read a stored "0", thus, resulting in a read upset. The ratio of the widths of the pull-down FinFET to the access FinFET commonly referred to as the cell ratio (CR) determines how high the "0" storage node rises during a read access [19].

The Cell Ratio (CR) 5 (W1/L1)/(W5/L5) is as shown in figure 2. Smaller cell ratios translate into a bigger voltage drop across the pull-down FinFET requiring a smaller noise voltage at the "0" node to trip the cell. During a read operation, the conducting access FinFET lies in parallel to the pull-up PMOS, lowering the gain of the static transfer characteristic and further decreasing cell immunity to noise.

3. Write Noise Margin

Write Noise Margin (WNM) is the maximum bitline (BL) voltage that is able to flip the state of the FinFET based SRAM cell while bitline bar (BL') voltage is kept high [19]. Higher the WNM, greater is the stability. Use of a weaker pull up (pFinFET) and a stronger access FinFET helps the node storing "1" to discharge faster, thus facilitating a quicker write of "0". The write margin can be measured as the maximum BL' voltage that is able to flip the cell state while BL is kept high. Hence, the write margin improves with a strong access and a weak pull up FinFET at the cost of cell area and the cell read margin.

5. 4.Power and Delay

Power dissipation of the FinFET SRAM cell assesses the utility of the cell in portable devices. The fundamental advantage of the FinFET based SRAM is in its low access time and power dissipation due to low SCE's and leakage current in FinFET device. While a strong driving current reduces the access time, it also increases the power dissipation in the SRAM cell. In SRAM, the propagation delay depends on the column height and wire delays. Thus segmentation is employed to reduce the delay. Since the power-delay-product is constant for a device, increasing one decreases the other and vice-versa. Upsizing the FinFET device in SRAM cell decreases the delay at the cost of slightly increased power dissipation. However to reduce power dissipation, leakage currents need to be minimized which warrant an increase in the channel length or higher transistor threshold voltages. Larger channel length results in higher delay and there exists a trade-off between these two performance indices.

III. MONTE CARLO ANALYSIS OF FinFET PROCESS VARIATION

The reason behind the observed random distribution of FinFET device parameters is due to the limited resolution of the photolithographic process which causes W/L variations in MOS transistors. The variations in W and L are not correlated because W is determined in the field oxide step while L is defined in the poly and source/drain diffusion steps. In FinFET based SRAM, the process parameters variation include FinFET width (Wfin), fin thickness (Tfin) and threshold voltage (Vth). These variations affect the noise margins, power consumption and delay. Memory designs are optimized for 6s variations [20]. To assess the impact of process parameters on FinFET SRAM, we carried out Monte Carlo simulation HSPICE.

IV.RESULT AND DISCUSSION

It can be seen that the high Static Noise Margin (SNM) reduces and low SNM increases with decrease in the width of load FinFET M2. Thus, as width of the load FinFET reduces, so does the driving capability of the load device. This implies that Q reaches to VOH at a much higher voltage, thus, resulting in a decrease in high SNM. It is further observed that as the widths of the pull-up device decreases, the switching threshold also tends to reduce. Since the driving capability of M2 reduces with the reduction in width, therefore, it requires lesser amount of voltage at BL' for the purpose of switching threshold.

The variation of Static Noise Margin (SNM) for driver FinFET M1 with variation of its width is increase in the width of driver FinFET M1, the high SNM reduces and low SNM increases. This is due the fact that the leakage current is considerably reduced due to increased controlof the FinFET device structure, resulting relatively in high Ion/Ioff ratio [21]. In the case of RNM, the stability of the cell is most seriously compromised as the node containing '0' is pulled up to a voltage determined by the relative sizing of driver and access FinFET's.

Table.1 Mean and Standard deviation of RNM Monte Carlo analysis

	Load	Driver	Access	All W
Mean(mV)	27.1390	27.1460	27.6201	28.0672
Stander Deviation (mV)	1.0501	1.0030	2.0875	2.9062

Table 2 Mean and Standard deviation of WNM Monte Carlo analysis

	Driver	Load	Access	All W
Mean(mV)	81.5366	81.5047	81.7485	65.6410
Standard Deviation (mV)	1.9654	2.4564	4.8751	4.9858

V.CONCLUSION

In this paper, we have analyzed different tradeoffs involved in the design of FinFET based SRAM and optimized the performance of the cell for robustness. The analysis of SNM, RNM, WNMload and driver have been carried out. Further, the effect of process variation on the SRAM cell performance was analyzed using Monte Carlo simulation on HSPICE. It was identified that while the relative levels of the noise margins were lower for the underlapped case, the standard deviation was considerably lower too. It was also found that smaller FinFET widths give rise tolarger deviations than larger ones. Thus in future FinFET SRAM based on minimum FinFET width, would be prone to process variations. The temperature dependence of noise margins and static power was also observed for FinFET based SRAM. While SNM and RNM decreased with increasing temperature, WNM increased. Since the stability of the FinFET based SRAM cell in the idle state is the most important metric, temperature effects have to be accounted for in design of memory circuits.

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