

# A New Technique to Improvement of Power and Delay on Various in Dynamic Circuits

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**Abstract** – The microprocessors in the modern era are propelled by high speed, small area and low power circuits. Dynamic logic circuits are used for high performance and high speed applications. Wide OR gates are used in Dynamic RAMs, Static RAMs, high speed processors and other high speed circuits. In spite of their high performance, dynamic logic circuit has high noise and extensive leakage which has caused problems for the circuits. To overcome these problems Domino logic circuits are used which reduce sub threshold leakage current in standby mode and improve noise immunity for wide OR gates. High noise sensitivity is the result of sub threshold leakage current that flows through the evaluation network. With the advancements in CMOS manufacturing process to scale down into the ultra deep sub-micron regime, the leakage current becomes an increasingly more important consideration in VLSI circuit design. According to the simulations in HSPICE at 90nm and 65nm CMOS technology, the proposed circuit shows the improvement of Average power consumption upto for 8 input OR gate 30% compared existing domino logics. This control circuit produces small voltage at the source of the pull down network in the standby mode. It improves the noise immunity of the domino circuits. The performance of these circuits has been evaluated by HSPICE using a BSIM4.

**Keywords-** Leakage current; Low Power, High Speed, CKD, UNG.

## I. INTRODUCTION

Wide OR gates are used in Dynamic RAMs, Static RAMs, high speed processors and other high speed circuits. Implementation of wide OR gate using static CMOS circuit requires large number of transistor and leakage power dissipation is also considerable [1].

While in comparison to static CMOS circuits, dynamic CMOS circuits have a large number of advantages such as lower number of transistors, low-power, higher speeds, short-circuit power free and glitch-free operation. Dynamic CMOS circuit technique [2] allows us to significantly reduce the number of transistors used to implement any logic function.

In spite of their high performance, dynamic logic circuit has high noise [3] and extensive leakage which has caused problems for the circuits. The main limitations of dynamic logic are cascading and charge sharing.

To overcome these problem domino circuits are use. In addition to dynamic logic an inverter and a weak pMOS pull-Up keeper transistor (with a small (W/L) ratio) is added to the dynamic CMOS output stage in domino logic. Inverter is use to avoid cascading problem and to avoid charge sharing problem weak keeper is used, which essentially forces high output level unless there is

a strong pull-down path between the output and the ground.

High fan-in [4] domino circuits are used to design high performance register files, ALU front ends, and priority encoders in content addressable memories. Wide domino logic refers to domino logic gates with N parallel pull down branches when N is greater than 4; that are used to design circuits in microprocessor critical path.

By scaling down the technology the sensitivity of the dynamic node to the noise sources has emerged as a serious design challenge.

For improving noise immunity and reducing leakage the keeper transistor is added. However, power dissipation increases and performance degrades by adding this pMOS keeper transistor.

Upsizing the keeper transistor improves robustness at a cost of higher power dissipation and delay. The severity increases many fold in wide Domino circuits because of higher number of parallel pull-down branches [38].

Therefore small size keeper is desired for high-speed applications while to increase the robustness, larger keeper is required. The keeper ratio  $K$  is defined as

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{keeper transistor}}{\mu_n \left(\frac{W}{L}\right)_{evaluation transistor}}$$

Where  $W$  and  $L$  denote the transistor size, and  $\mu_n$  and  $\mu_p$  are the electron and hole mobility, respectively. However, the traditional keeper approach is less effective in new generations of CMOS technology. Although keeper upsizing improves noise immunity, it increases current contention between the keeper transistor and the evaluation network. Thus, trade off exist between delay and power to improve noise and leakage immunity.

The dynamic logic circuit requires two phases. The first phase, when clock is low, is called the pre-charge phase and the second phase, when clock is high, is called the evaluation phase. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs  $A$  and  $B$ ). The capacitor, which represents the load capacitance of this gate, becomes charged [1-2]. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase as shown in Fig.1.

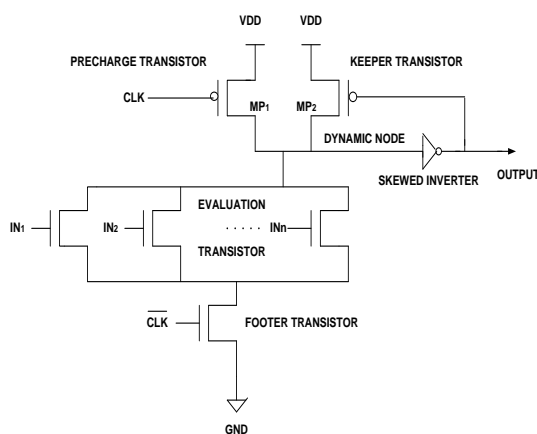


Fig.1 Footed domino logic circuit.

During the evaluation phase clock is high. If inputs  $A$  and  $B$  are also high, the output will be pulled low. Otherwise, the output stays high (due to the load capacitance).

Dynamic logic has a few potential problems that static logic does not. For example, if the clock speed is too slow, the output will decay too quickly to be of use. Also, the output is only valid for part of each clock cycle, so the device connected to it must sample it synchronously during the time that it is valid[3-4]. Also, when both  $A$  and  $B$  are high, so that the output is low, the circuit will pump one capacitor-load of charge from supply to ground for each clock cycle, by first

charging and then discharging the capacitor in each clock cycle.

This makes the circuit (with its output connected to a high impedance) less efficient than the static version (which theoretically should not allow any current to flow except through the output), and when the  $A$  and  $B$  inputs are constant and both high, the dynamic NAND gate uses power in proportion to the clock rate as long as it functions correctly [5].

The power dissipation can be minimized by keeping the load capacitance low, but this in turn reduces the maximum cycle time, requiring a higher minimum clock frequency; the higher frequency then increases power consumption by the relation just mentioned. Therefore, it is impossible to reduce the idle power consumption (when both inputs are high) below a certain limit which derives from an equilibrium between clock speed and load capacitance.

## II. LITREATURE SURVEY

Dynamic logic is over twice as fast as normal logic; it uses only fast N transistors. Static logic is slower because it uses slow p-type transistors to compute logic. Dynamic logic is harder to work, but if we need the speed there is no other choice.

Dynamic logic requires two phases, the first phase is set up phase or pre-charge phase, in this phase the output is unconditionally go to high (no matter the values of the inputs).The capacitor which represents the load capacitance of this gate becomes charged.

During the evaluation phase, CLK is high. Popular implementation of dynamic logic is domino logic. Domino logic is a CMOS based evaluation of the dynamic logic techniques which are based on the either PMOS or NMOS transistors. It was developed to speed up the circuits.

The dynamic gate outputs connect to one inverter, in domino logic. In domino logic, cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to 1 (until the next clock cycle) just as dominos, once fallen, cannot stand up. The structure is hence called domino CMOS logic.

### 1. Basic Working Principal

The domino CMOS circuit shown has two modes of operation as shown in the Fig.1.

- Pre-charge phase,
- Evaluation phase.

### 2. Pre-charge phase

This happens when clock signal is low. Thus the NMOS pull-down network is turned off [3]. The clock

controlled PMOS transistor is turned on. So the output node is charged to  $V_{DD}$ . Hence this is called pre-charge phase or setup phase.

### 3. Evaluation phase

This happens after the pre-charge phase and when the clock signal is high [5]. The output nodes are either pull down or pull up depending on the inputs to the NMOS transistors. This defines the operation of the dynamic CMOS circuit.

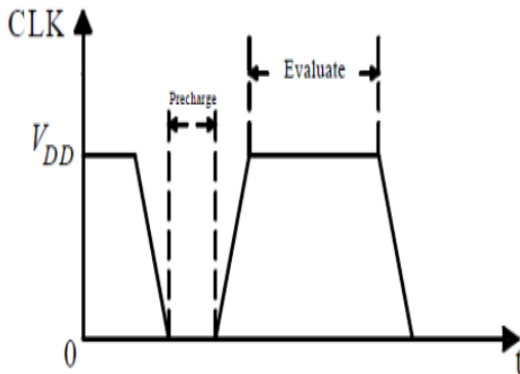


Fig.2 Waveform Of The Clock Needed To Operate Domino Logic Circuit [6].

Domino logic is the most popular dynamic logic. It runs 1.5-2 times faster than static CMOS logic because, dynamic gates present much lower input capacitance for the same output current and a lower switching threshold. Domino circuits are in function very similar to the clocked CMOS circuit.

In Domino logic a single clock is used to pre-charge and evaluate a cascaded set of dynamic logic blocks. During the pre-charge phase ( $CK=0$ ) all output nodes all (N) of the dynamic gates are pre-charged to high, as shown in Fig.1 through the PMOS transistor, and thus the outputs of the corresponding buffers are pre-charged to low.

Since all transistors of subsequent dynamic gates are fed from such buffers, these will be turned off during the pre-charge phase.

### 4. Conventional- Keeper Domino Logic

Due to their high speed and low device count especially compared to complementary CMOS, dynamic logic circuits are used in a wide variety of applications including microprocessors, digital signal processors, and dynamic memory As shown in the Fig.3, At first, consider the footless standard domino logic (FLSDL).

In standard domino logic gates, a feedback keeper transistor is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and sub-threshold leakage current [10].

The keeper transistor is fully turned on at the beginning of evaluation phase, then the keeper transistor and

evaluation network compete to determine the logical state of the dynamic node. This contention between the keeper transistor and the pull down network degrade the circuit speed and power characteristics.

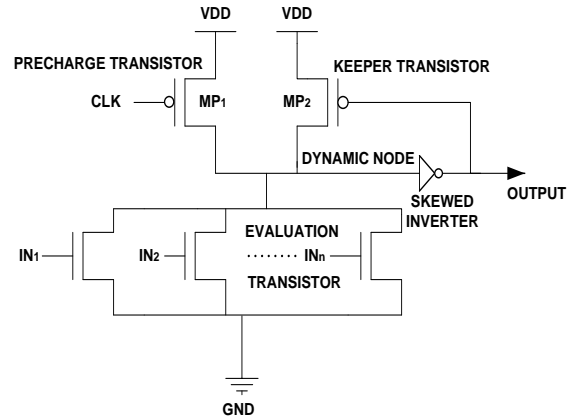


Fig.3 Footless Standard Domino Logic (FLSDL) [10].

The footless standard domino circuit works as follows: when clock is low, the circuit is in pre-charge mode. The dynamic node starts to go high through  $MP_1$  and  $MP_2$ . The output node goes low, and then the  $MP_2$  device is turned on. Therefore, it causes faster charging in dynamic node.

When clock is high,  $MP_1$  is off; hence the circuit has two states, standby mode and active mode. The standby mode is when all inputs to evaluation network devices are low. In fact, in this mode all input signals applied to pull down network are at zero, so the dynamic node remains high, but due to sub-threshold leakage current, the dynamic node encounters some discharging.

The dynamic node waveforms for  $OR_4$  and  $OR_8$  (same as  $IN_4$  and  $IN_8$ ) gates. The output waveform is affected by noise applying to the evaluation network. If we upsize the transistors of evaluation network, the speed increases but the noise margin will be decreased. Upsizing the keeper transistor increases the contention between keeper transistor and evaluation network. Conventionally, the robustness of standard domino circuit can be improved by upsizing the keeper transistor [11].

The second standard technique is footed standard domino logic (FSDL) as shown in the Fig. 4. This circuit's treatment is look like the footless domino logic style. However because of the stacking effect in FSDL, the speed of logic is lower than footless one, but the noise immunity is higher. When clock is low, the dynamic node is pre-charged to  $V_{DD}$ . In this phase the footed transistor is turned off.

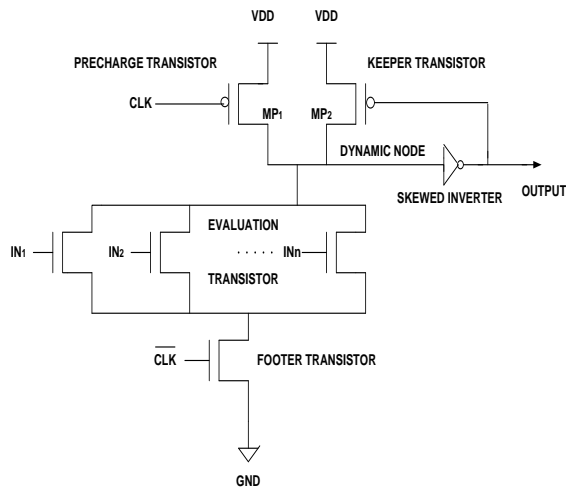


Fig. 4 Footed Standard Domino Logic (FSDL) [10].

This leads to one of the two following cases depending on the value of the strong keeper current; if the current of the NMOS transistor in the PDN is larger than that of the strong keeper, then the dynamic node will discharge very slowly resulting in very low speed for the circuit.

On the other hand, if the current of the NMOS transistor in the PDN is smaller than that of the strong keeper, then the dynamic node will not discharge at all in this case resulting in an erroneous output for the circuit and excessive power consumption.

### 5. High speed Domino logic circuit

High speed domino is another domino logic circuit. In domino logic circuit current drawn through the keeper transistor and pull down network NMOS transistors at the beginning of the evaluation phase, can be reduced by applying a clock delay in the circuit. That does not affect the leakage current in the circuit as shown in Fig.2.

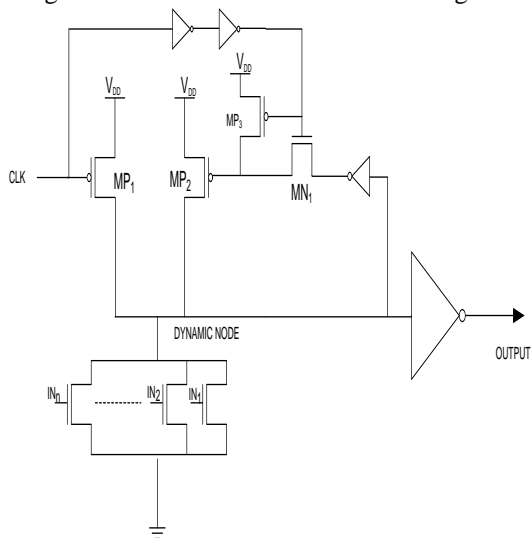


Fig.5 High speed domino logic circuit.

But apart from this the extra clock delay consumes extra area and power, which is a big drawback of the circuit. It gives an effective solution to increase the robustness of the circuit.

In High speed domino logic circuit when clock becomes high,  $M_{n1}$  is still off and  $M_{p2}$  is still on. Therefore  $M_{p2}$  turns off the keeper transistor. After some delay of inverter  $M_{p2}$  becomes off. Now if dynamic node remains high during the evaluation phase, NMOS is turn on which turns on the keeper transistor.

Hence at the beginning of evaluation phase dynamic node is afloat, so in the absence of keeper transistor, evaluation node may be discharged for any noise at the input section. Also the voltage at the gate of the keeper transistor would be  $V_{DD} - V_{thn1}$ . This would provide a dc current flow through the PMOS keeper transistor and the NMOS network.

### III. PROPOSED WORK

The proposed circuit here is implemented in 65 nm HSPICE CMOS technology with the power supply of 1V. Our circuit is based on footed domino logic circuit and based on this the proposed circuit is given which is having better leakage tolerance and improved noise immunity. The circuit is shown in figure (4) and has been tested for 8 and 16 inputs OR gate. To operate the circuit basically we have two modes of operations, namely precharge mode and evaluation mode.

During precharge phase, the the dynamic node of all the gates are charged to VDD, which also causes the inverter output to go to 0 V. Now during the evaluation phase the logic signal associated with the pull down network is evaluated and the inverter output perhaps changes from 0 to VDD or some inverter output may remain at ground depending upon the logic signal provided to the pull down network. In the proposed circuit an NMOS is added as shown in Fig.6.

The main function of this transistor is to draw the contention current of the PMOS keeper and also it helps to speed up the discharging process of the capacitor at the dynamic node. At the beginning of the precharge mode the precharge device is in active mode. Therefore the voltage at the dynamic node will be at 0 V and hence that will pass through an inverter so the output at the inverter will be VDD.

In consequence the extra added transistor will turn on and at the beginning of the precharge phase there will be contention of current between the two current derived from the extra added transistor and the keeper transistor because the precharge device tries to charge the capacitor CL and the current due to the added NMOS tries to discharge the capacitor CL.

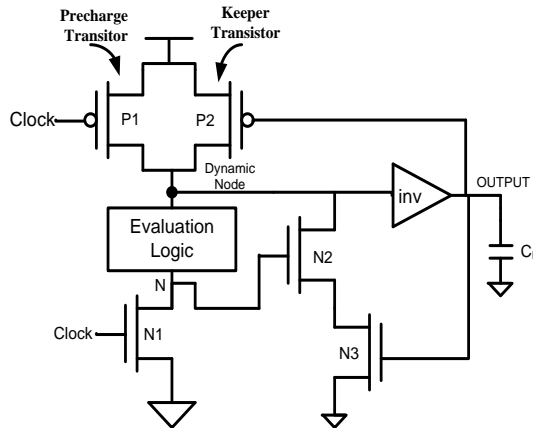


Fig.6 Proposed Diode Footed Domino Circuit.

The transient response of the conventional footer less domino logic is shown in Fig.7. in which output depends on the clock it gives same wave form as clock signal due to inverting the output signal. there is only one keeper to maintain the charge in dynamic node and make contention free between the keeper and pull down network.

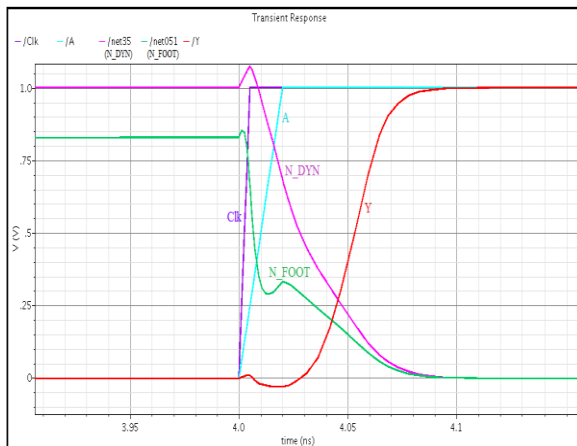


Fig.7. Output transient response of proposed domino circuit.

#### IV. SIMULATION AND RESULTS

The circuits were simulated with using HSPICE TOOL using 65nm and 90nm technology using 1V and 1.2V. The circuit was being compared with the OR gate previous techniques. The OR gate was implemented because it is a typical example of wide pull-down network.

The proposed circuit was being implemented for OR gate and being compared with the OR gate of other reference circuits and also investigated with different values of fan-in. It was found that the proposed circuit

performs better than the previous proposed circuits. The simulation has been performed for proposed circuits and reported circuits. We have evaluated the leakage power consumption, active mode power consumption A.C noise margin of the proposed designed topologies and the comparisons have also been made with the reported circuits by performing simulation using 0.065- $\mu$ m CMOS technology.

Some parameters of the proposed circuit such as delay, average power, unity noise gain are calculated (Table II) for 8 input OR gate. In the proposed circuit we find improvement in these parameters as compare to the previous domino logic circuit. The comparison of unity noise gain of the proposed circuit with other standard domino logic circuit is shown in Table II and II.

Table III shows the comparison of 16 input OR gate proposed circuit with footed domino logic circuit, footless domino logic circuit, high speed etc. domino logic circuit. The circuit is simulated at 65nm and 90nm technology in cadence spectre at 1V. For 8 and 16 input fan in OR gate comparison between well known existing circuit design techniques, we performed several simulations to obtain UNG and dissipated power as shown in the table. The simulation is performed by setting  $M_{keeper} (W/L) = .25u$ , PMOS  $(W/L) = 5u$ , NMOS  $(W/L) = 2.5u$  and  $C_L = 1pf$ .

Table.1 At 65nm Process Technology  $V_{dd} = 1$  v, For 8Input OR Gate.

Parameters	FLD	FD	HSD	CKD	DFD	LC R	CC D	Proposed Circuit
Power ( $\mu$ W)	2.586	3.697	277.0	138.4	4.144	2.670	2.386	2.445
Normalized power	1	1.43	107.36	53.51	1.60	1.03	0.922	0.945
Propagation delay (ps)	18.41	36.44	18.34	20.06	32.61	18.43	19.01	18.91
Normalized propagation delay	1	1.97	0.99	1.08	1.77	1.00	1.032	1.027
Power delay product (pJ)	47.60	134.4	5080	2776	135.1	49.20	44.02	46.23
UNG	0.325	0.365	0.331	0.357	0.369	0.376	0.387	0.394
Normalized UNG	1	1.123	1.01	1.09	1.13	1.15	1.190	1.21
No. of transistors	20	21	26	31	24	22	31	27

Table.2 Simulation is done with  $V_{dd}=1V$ , Frequency is 100MHz, For 16 Input OR Gate At 65nm Process Technology.

Parameters	FLD	FD	HSD	CKD	DFD	LCR	CCD	Proposed Circuit
Power ( $\mu W$ )	3.010	5.033	375.40	206.7	5.337	3.067	2.781	2.913
Normalized power	1	1.672	124.71	68.67	1.77	1.01	0.923	0.967
Propagation delay (ns)	20.57	42.88	20.41	22.69	36.92	20.68	21.93	20.74
Normalized propagation delay	1	2.08	0.99	1.10	1.79	1.00	1.066	1.00
Power delay product (pd)	61.91	215.8	7661.9	4690.0	197.04	63.42	60.98	59.25
UNG	0.344	0.391	0.346	0.382	0.393	0.401	0.431	0.452
Normalized UNG	1	1.13	1.00	1.11	1.14	1.16	1.25	1.311
No. of transistors	20	21	26	31	24	22	31	27

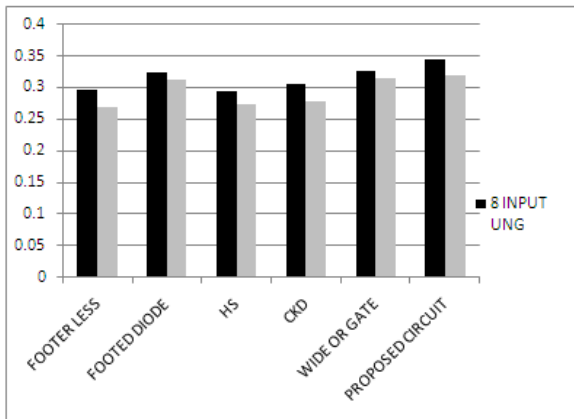


Fig.8 Comparison of UNG for 8 and 16 Input OR gate.

Table.3 Comparison of Area (No. Of Transistor).

S. No.	Logic Style	8 Input	16 Input	32 Input
1.	SFLD	12	18	34
2.	FLD	13	21	37
3.	HSD	18	26	42
4.	CKD	23	29	45
5.	WFD	16	24	40
6.	LCR	15	23	39
7.	CCD	20	28	36
8.	Proposed Circuit	15	23	31

## V. CONCLUSION

Sub threshold and gate oxide leakage currents need to be suppressed in a 65nm CMOS technology. In this paper, a new circuit is proposed to reduce both subthreshold and gate oxide leakage currents simultaneously. Proposed circuit employs a PMOS sleep switch transistor between the power supply and output node with dual threshold voltage CMOS technology to suppress both subthreshold and gate oxide leakage currents. The sleep transistor, source of the pull-down network and source of NMOS transistor of output inverter is control by additional sleep signal. The simulation has been done using HSPICE software for OR8 and OR16 gates at 25°C. The proposed circuit reduces the total leakage power consumption upto 99.41% and 99.51% as compared to the standard dual threshold voltage footless domino circuits at 25°C and 110°C, respectively. Proposed circuit reduces the total leakage power consumption upto 93.79% and 97.98% as compared to the sleep control techniques at 25°C and 110°C, respectively.

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