

Novel Forced Stack based Power-on-Reset circuit for low energy application

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Abstract- This novel article describes both the function of Power-on Reset (POR) and the strategies for low energy application, when used with dual-supply SoC's. The article demonstrates why to avoid discrete PORs and PORs internal to processors. It concludes with explanations of voltage sequencing, voltage tracking, and reset sequencing. Design of a low-energy power-ON reset (POR) circuit is proposed to reduce the energy consumed by the stable supply of the dual supply static random access memory (SRAM) using FET devices, as the other supply is ramping up. The proposed design is based on stacking of pull-up and pull-down transistor in push-pull output stage also called sleepy approach to reduce the energy consumption of POR circuit. Proposed design offers $0.1735\mu\text{s}$ delay which is 8.2% lower than POR-LE while offers 1.2% higher power dissipation than POR-LE. But the multiplication of power and delay (is also called energy) is 7% smaller than POR-LE.

Keywords- POR, activation time, wake-up time, sequencing.

I. INTRODUCTION

A power-on reset (PoR) is a circuit that provides a predictable, regulated voltage to a microprocessor or microcontroller or embedded SoC's with the initial application of power. The PoR system ensures that the microprocessor or microcontroller will start in the same condition every time that it is powered up. A PoR system can be a peripheral, but in sophisticated processors or controllers the PoR is integrated on the main chip [1, 2].

The most basic PoR system can comprise a resistor and capacitor connected together with values tailored so that, when power is first applied, the capacitor takes a predictable and constant time to charge up. For computer use, however, additional components are often required, including a circuit called a Schmitt trigger. When the PoR circuit is designed, the charge-up time should be adjusted by trial and error so that all of the processor or controller circuits can set them to the correct initial values before the computer begins to function.

A well-designed PoR circuit can ensure that when power is applied to a computer, it will start up properly every time (or almost every time), and will never (or rarely) freeze up right away. This feature not only saves the user a great deal of frustration, but it offers a last resort in case of a stubborn system crash the so-called cold boot, where the computer is completely powered-down for a minute or two, and then powered-up all over again.

In VLSI devices, the power-on reset (PoR) is an electronic device incorporated into the integrated circuit that detects the power applied to the chip and generates a reset impulse that goes to the entire circuit placing it into

a known state [3, 4]. A simple PoR uses the charging of a capacitor, in series with a resistor, to measure a time period during which the rest of the circuit is held in a reset state. A Schmitt trigger may be used to desert the reset signal cleanly, once the rising voltage of the RC network passes the threshold voltage of the Schmitt trigger.

The resistor and capacitor values should be determined so that the charging of the RC network takes long enough that the supply voltage will have stabilised by the time the threshold is reached [5, 6].

One of the issues with using RC network to generate PoR pulse is the sensitivity of the R and C values to the power-supply ramp characteristics. When the power supply ramp is rapid, the R and C values can be calculated so that the time to reach the switching threshold of the Schmitt trigger is enough to apply a long enough reset pulse.

When the power supply ramp itself is slow, the RC network tends to get charged up along with the power-supply ramp up. So when the input Schmitt stage is all powered up and ready, the input voltage from the RC network would already have crossed the Schmitt trigger point. This means that there might not be a reset pulse supplied to the core of the VLSI.

The rest of this brief is organized as follows. Literature review part is discussed in Section II. The details of proposed SCDM based three-input XOR is discussed in Section III. Simulation results are analyzed in Section IV. Finally, the conclusions are drawn in Section V.

II. LITERATURE REVIEW

This section covers the literature of various existing PoR Circuits. The A power-on reset pulse generator for low voltage applications (POR-PG)[7], Zero steady state current power-on-reset circuit with brown-out detector (POR-ZSS)[8], A sequence independent power-on reset circuit for multi-voltage systems (POR-SI)[9] and Low-Energy Power-ON-Reset Circuit for Dual Supply SRAM (POR-LE) [10]. Many papers on leakage power reduction using variation in circuit topology has been published now [11-13].

The forced stack technique is used to improve the performance of CMOS circuit. This technique reduces leakage power dissipation using transistor stacking.

Transistor stacking exploits the stack effect; the stack effect results in substantial sub threshold leakage current reduction when two or more stacked transistors are turned off together. Narendra *et al.* study the effectiveness of the stack effect including effects from increasing the channel length.

1. POR-PG

An on-chip power-on reset pulse generator (POR-PG) is used to determine the initial state of the memory devices of the system large scale integration circuit only.

This paper describes a POR-PG for low power voltage supply (V_{dd}) Hardware measurement proves improved pulse height relative to various power-on profiles and process fluctuations. Further, the design provides robust noise immunity against voltage fluctuations on the power supply line.

The circuit is implemented within a small area ($115\mu\text{m} \times 345\mu\text{m}$) in the input/output buffer area of a micro-processor and hard disk controller integrated LSI with $0.25\text{-}\mu\text{m}$ four-layer-metal CMOS technology.

A Power-on reset pulse generation circuit for low voltage application is proposed. This circuit improves pulse height and noise immunity compared with prior circuits considering process, temperature, and voltage variations.

The circuit is implemented in small area in the input/output* buffer area of an integrated LSI of a microprocessor and a hard-disk controller for the internal power supply voltage of 2.511 and 1.8V with $0.25\text{-}\mu\text{m}$ CMOS technology.

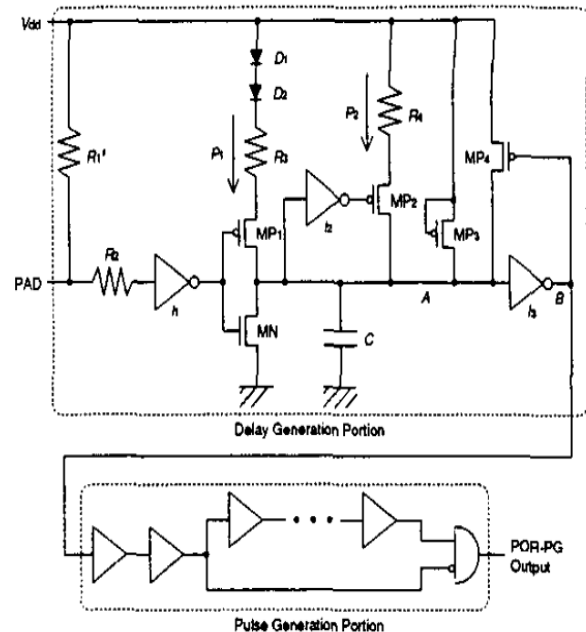


Fig.1 Power-On-Reset using Pulse Generation Portion.

2. POR-ZSS

A novel Power on reset (POR) circuit with Brown out (BO) detector having zero steady state current consumption is proposed. The circuit has been designed in 65nm CMOS process at a single supply of 1.1V. Both the POR and BO thresholds are independently adjustable in the circuit. Simulation results show that the POR threshold does not depend upon the supply ramp-rate at fixed process and temperature corner. BO circuit works for a large range of supply ramp down rates. Due to zero steady state current consumption, the proposed circuit is well suited for low power applications.

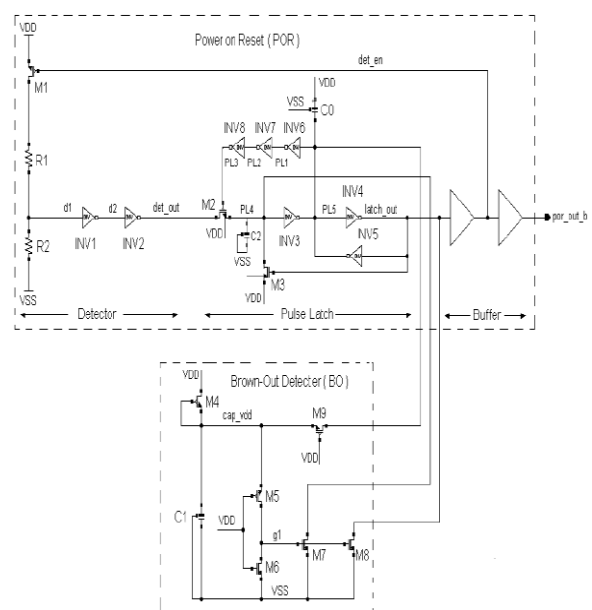


Fig.2 Proposed POR and BO detector circuit.

3. POR-SI

With the advent of multiple supply domains on a single chip, issues related to power sequencing are becoming a major hurdle for system designers. Existing POR strategies fail to cope up with these issues. We propose a scheme in which the power on reset generation is independent of the sequence of supply ramp-up.

The circuit implementation of the proposed methodology has been realized for a dual supply system. The basic circuit is modified so as to consume zero static current. An attempt to reduce any leakage current during supply ramp-up has also been made successfully. Simulation results verify the sequence independence concept and low power consumption. Further the proposed realization is modular enough to be extended for more number of supplies

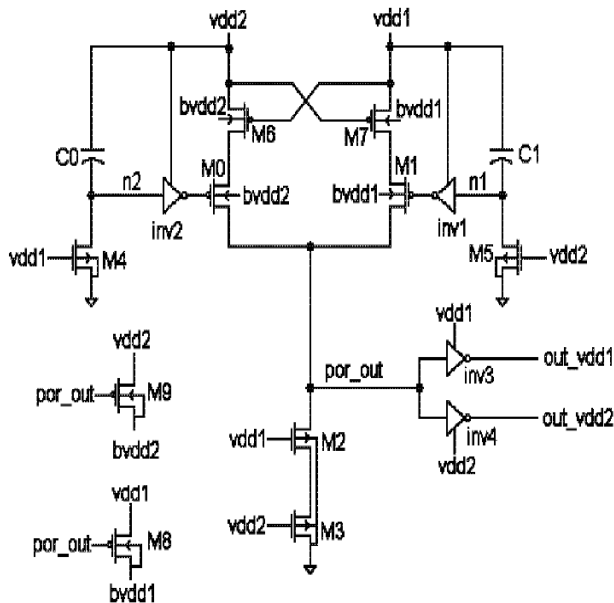


Fig.3 Dual Supply POR with Ultra low current consumption.

4. POR-LE

Design of a low-energy power-ON reset (POR) circuit is proposed to reduce the energy consumed by the stable supply of the dual supply static random access memory (SRAM), as the other supply is ramping up. The proposed POR circuit, when embedded inside dual supply SRAM, removes its ramp-up constraints related to voltage sequencing and pin states. The circuit consumes negligible energy during ramp-up, does not consume dynamic power during operations, and includes hysteresis to improve noise immunity against voltage fluctuations on the power supply. The POR circuit, designed in the 40-nm CMOS technology within 10.6- μm^2 area, enabled 27 \times reductions in the energy consumed by the SRAM array supply during periphery power-up in typical conditions.

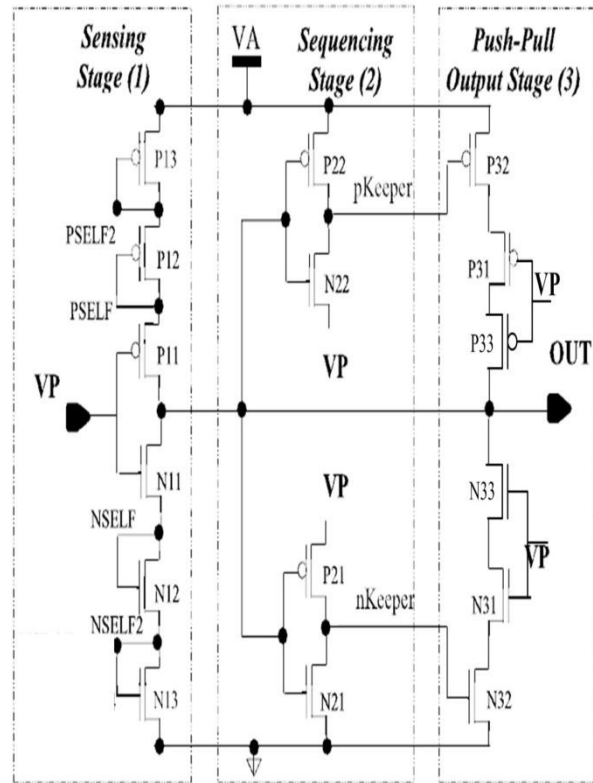


Fig.4 Proposed Forced stack based POR circuit.

III.RESULT ANALYSIS

We designed and implemented the novel modified POR circuit using forced stack topology in the 45-nm CMOS technology using 16 Transistor. Table-1 shows the simulation result absolute value and Fig. 6 shows the simulation result for the proposed design.

We used silicon qualified SPICE models to simulate the netlist along with parasitics, at extended corner lot points of the process for nMOS (N) and pMOS (P) temperature 25 °C and VDD=1Volt using SPICE EDA Tool. POR can be characterized on the basis of following parameters such as wake-up time, power dissipation, Energy and Transistor count.

The proposed technique is compared with the new existing technique POR-LE[10]. The proposed design is based on stacking of pull-up and pull-down transistor in push-pull output stage also called sleepy approach to reduce the energy consumption of POR circuit.

Proposed design offers 0.1735 μs delay which is 8.2% lower than POR-LE while offers 1.2% higher power dissipation than POR-LE. But the multiplication of power and delay (is also called energy) is 7% smaller than POR-LE.

Table-1 Result Analysis of POR circuit at 45nm technology and 1Volt.

Design Parameter	POR-LE	Proposed
Wake-up Time (μsec)	0.189	0.174
Avg Power Dissipation (μW)	2.157	2.184
Energy ($\times 10^{12}$ Jule)	0.408	0.379
Transistor Count	16	16

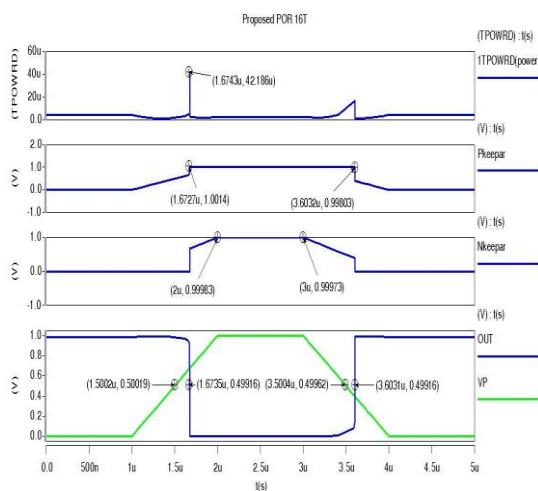


Fig.5 Simulation result of proposed design at 1 Volt.

IV. CONCLUSION

We can use proposed POR with the state-of-the-art POR in analog and digital domain. From Table-1, it is evident that our circuit has a significantly low delay advantage as compared to POR-LE. We have presented the design of a novel 16 Transistor power-ON circuit to reduce the energy consumed during supply ramp-up in a dual supply SRAM. The circuit implementation in the 45-nm CMOS technology occupied same area as POR-LE. The proposed design is based on stacking of pull-up and pull-down transistor in push-pull output stage also called sleepy approach to reduce the energy consumption of POR circuit. Proposed design offers 0.1735 μs delay which is 8.2% lower than POR-LE while offers 1.2% higher power dissipation than POR-LE. But the multiplication of power and delay (is also called energy) is 7% smaller than POR-LE.

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