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A Novel Low Power 11T SRAM Design Cell in Nanometer Regime

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Abstract- **Now a day's low power SRAMs have become a critical component of many VLSI chips. This has especially true for microprocessors, where the demanding on chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processors and the main memory. Simultaneously, power dissipation has been becoming an important factor to recognise due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated applications. This proposed 11T SRAM has been compared with standard 6T SRAM and existing 9T SRAM (with bit-interleaving capability) in term of Power consumption, Delay and Power Delay Product (PDP) at various supply voltages as 1.8V, 1.6V and 1.4V. For the stability analysis SNM (Static Noise Margin) also analyzed at the supply voltage 1.8V. The proposed 11T SRAM proves to be better in terms of power and PDP at all the supply voltages. At 1.8V power saving by the proposed design is 73.88% and improvement in PDP is 71.53% compared to standard 6T SRAM cell and significant improvement is observed at other supply voltages also. In term of stability the proposed design proves better as compare to existing circuits.**

Keyword- **6T SRAM cell, 11T SRAM cell, 9T SRAM cell, MTCMOS, Low Power Consumption**

I. INTRODUCTION

SRAM memories are most essential element of any digital circuit. To store one bit data in SRAM cell minimum six transistors (6T) are required. Dynamic random access memory (DRAM) circuit is very simple compare to SRAM cell. In basic DRAM cell minimum only one transistor and a capacitor is required to stored single bit.

The main advantage of DRAM over SRAM is its structural simplicity i.e. SRAM required six transistor but DRAM contains one transistor and one capacitor only. The read operation in the DRAM cell is more difficult and complex than the write operation. In this, read involves discharge of the initially capacitor with charge. So after every read operation the capacitor need to be charged. Every bit stored in SRAM with six transistors. This chapter means introduction part of thesis consists of discussion of the motivation, about different type of memories and overview of the thesis.

SRAM is an important part of register file to determine its overall performance of memories. But in Deep Submicron Tech (DSM) as the size of the transistor is scaling down in nanometer technology. The issue of leakage power is most common in SRAM cells which are designed for a low power application. As a result the power consumption in SRAM design becomes a most common issue. But in low power design the speed of circuits degraded. So to optimize low power circuit without compromising with speed becomes the major concern of modern very large scale integration (VLSI) design. Furthermore due to scaling the circuit designs also faces design challenges for the circuit design for low power. The scaling causes the reduction in threshold voltage. For low Vth and ultra-thin gate oxide leads to the leakage power consumption [1]. The stability of the cell during read, write mode is also affected [2].

The supply voltage scaling becomes most effective technique for power saving. The scaling of supply voltage reduces the power consumption of the circuit in good amount [3]. But due to scaling of supply voltage and device size of SRAMs it affects process variation parameters and threshold voltage together. This leads to reduction in Static Noise Margin (SNM) that degrades cell stability [9, 10].

The static noise margin is linearly dependent on the supply voltage. The supply voltage is scaled down to reduce power consumption the stability of SRAM cell is affected. Hence to get low power SRAM design while maintaining the cell stability becomes the main theme of SRAM designs in modern scenario. In this thesis the 11T and 13T SRAM cells have been proposed with bit interleaving capability with better performance. Other design of SRAM cells with bit interleaving capability are presented in [4-8] in past.

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1. Why SRAM?
The SRAM Array required more area of chip, since six transistors is required to store single bit. The SRAM, static RAM is more preferred compare with DRAM due to its high speed of operation. SRAM need not to require the data refreshment periodically. In case of Dynamic Random Access Memory (DRAM) requires the data refreshment periodically since it has a transistor and a capacitor in its structure. The refreshment is required in DRAM for data to remain valid. All the conventional SRAM cell is shown in Figure.1.

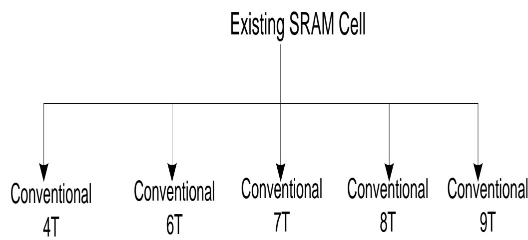

Fig.1 Flow diagram of Existing SRAM Cell

The brief overview of this paper as follows, in section 2 we have discussed literature review i.e. standard 6T SRAM and existing 9T SRAM cell for bit-interleaving capability has been discussed. Section 3 consists of elaboration of the proposed work, section 4 contains the simulation and results discussion and section 5 consists of conclusion part.

II. LITERATURE REVIEW

1. Conventional 6T SRAM Cell
The Conventional 6T SRAM cell has combination of six transistors in which four transistors (N1 P1, N2 P2) formed two inverters. These two inverters are back to back connected in cross coupled manner, apart from this two access NMOS transistors N3 and N4 acting as pass transistors and two data storing nodes (Q and QB).

These data storing nodes are accessed by the pass transistor N3 and N4 as shown in Fig.1. These cross-coupled inverters forming the latch, i.e. each bit is stored in the latch. The access transistors are enabled using Word Line (WL). When the Word Line (WL) is low, access transistors are disabled and cell works in hold state, at this time read or write operations cannot be performed, at this state latch can hold bit as long as the voltages remain at V_{dd} and GND. When the word line becomes high, access transistors N3 and N4 are enabled, and at this stage read and write operations can be performed [5]. Data is write at node Q through bit line and opposite data is stored at the node QB.

The 6T SRAM cell is used shared word-line architecture though this technique is simple and commonly used to arrange array of cell. The main disadvantage of this architecture is that the multi-bit soft error is very high since the adjacent bit share a WL each other. Apart from this 6T SRAM cell has read failure which is overcome in [11], write 1 failure [12] and also consume more power. Apart from this the standard 6T SRAM cell has been found to be rather unstable for deep submicron scale technology. This cell fails to meet the so many operational requirements due to the low read static noise margin (SNM).

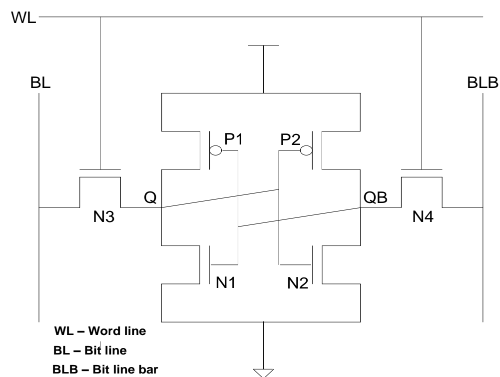

Fig.2. Conventional 6T SRAM cell

2. Existing 9T SRAM cell
In 9T SRAM cell three extra transistors N5, N6, P3 are added. Transistor N5 is connected between node Q and N1 for the data protection during read operation [11] , this transistor prevent the discharging of node Q since it turn off during read , write operation .

Transistor (N6, P3) forms a special inverter for AND logic operation [10] to activate local word line (LWL). It also have bit line (BL) ,world line (WL) and provide extra word line (RWL) for read operation , bit line CBLB to control transistor N5 as shown in Fig. 2 .

This 9T SRAM cell is designed with bit interleaving capability for soft error protection and this design also sort-out the problem of write 1 failure which was occurring in 6T SRAM cell. Also exhibit considerable improvement in write ability, read robustness, lower write and leakage power consumption, as well as has better

Fig. 2. 9T SARM cell

Tolerance in process variation [12]. Still average power and speed of the circuit can be further improved by connecting some extra transistor which is done in the proposed 11T circuit.

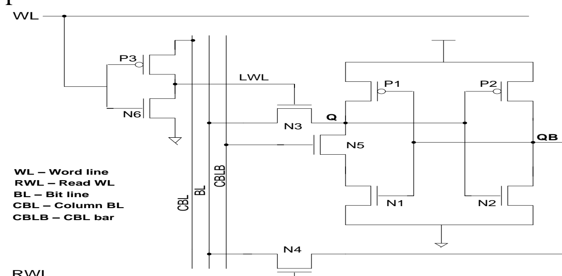

Fig. 3. 9T SARM cell

III. PROPOSED DESIGN

1. Proposed 11T SRAM cell

Single ended 11T SRAM cell for bit interleaving application has been proposed, the bit interleaving idea originate from the differential 8T SRAM cell [10]. Subsequently this idea is used in read disturb free 9T SRAM cell [12]. The working of the proposed cell is a little bit similar to the 9T SRAM cell less power consumption, high speed, less PDP. The proposed SRAM cell consist of eleven transistors seven NMOS from N1 - N7 and four PMOS from P1-P4 shown in Fig. 3.

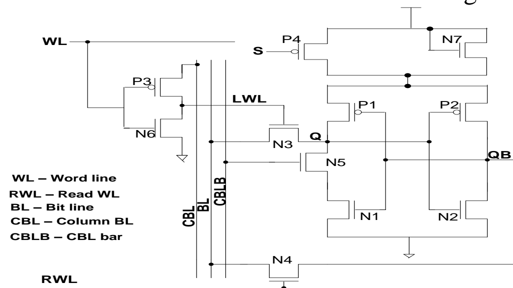

Fig.4. Proposed 11T SRAM cell.

In the proposed circuit two extra transistors P4 and N7 are connected to improve the cell performances. The transistor N7 is for reducing supply voltage and transistor P4 is work as switching transistor.

The operation principle of the proposed 11T SRAM cell is discussed below.

1. **Hold mode:** In hold mode, set the word line (WL) at high voltage while RWL signal switch low, hence transistor N3 & N4 turn off to prevent the access of bit line, CBLB is set high to turn on transistor N5 as a result data retention is afforded by the cross coupled back-to- back pair .
2. **Write Mode:** In write operation pull down WL at low and enable CBL signal, then LWL signal is pre-charged to high value as a result the data is written from bit-line (BL) to storage nodes (Q & QB) through N3 .
3. **Read mode:** During read mode first of all BL is set to high , then the special read word line (RWL) signal start read operation , CBL turns high and the CBLB is turn to low voltage and WL remains at high . From simulation result we will observed that proposed 11T SRAM cell generates Q and QB output which has proper logic without delegation of output waveform. The output waveform for proposed 11T SRAM cell is shown in Fig. 4.

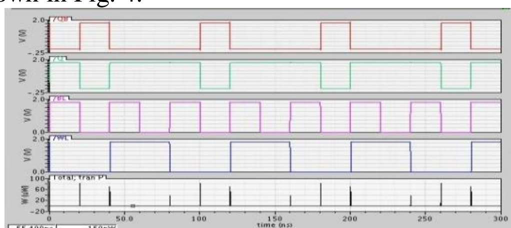

Fig.5. Output Waveform of Proposed Circuit.

2. Bit-interleaving and shared word line architectures

Mainly two ways are used to arrange the words in SRAM architecture. Shared word line shown in Fig. 5(a) and bit interleaving shown in Fig. 5(b). In the share word line architecture, all the bits of the same words are located next to each other clearly shown in figure.

This design is widely used because of its simplicity and compactness, since bits are adjacent to each other, the probability of multi-bit soft errors is very high. To solve the problem of soft errors bit interleaving architecture is used. A detailed explanation of these techniques is given in [10].

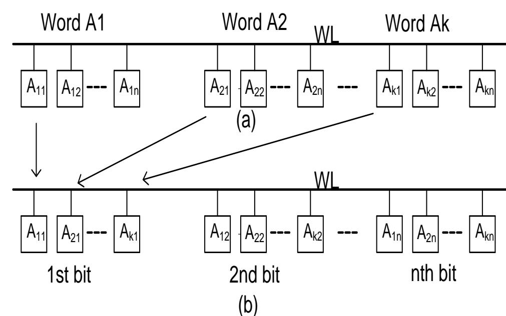

Fig.6. SRAM word organization (a) Shared word line (b) Bit-interleaving.

Bit-interleaving is commonly used in SRAM design, to provide soft error protection as well as area efficient utilization of wiring. Fig. 6 shows 2x2 bit-interleaving architecture of proposed 11T SRAM cell. The detail explanations and the working of 2x2 bit-interleaving architecture is given in [12].

IV. CELL PERFORMANCE ANALYSIS

In this section, cell properties such as SNM, Speed, Power consumption, PDP etc. are compared with the existing design, namely the standard 6T cell and 9T cell. All the existing and proposed circuit is simulated in Cadence Virtuoso at 180nm technology at frequency 25 MHz Power consumption and delay is calculated at various supply voltages 1.8V, 1.6V and 1.4V respectively.

We observed that as we scale down the supply voltage the power consumption of the SRAM cell also reduces. The size (W/L ratio) of the transistors (N-CMOS and P-CMOS respectively) is taken to be the same for all transistor of the cell to compare different type of SRAM cell.

1. Speed and power analysis

The proposed SRAM cell shows 73.88% reduction in power , 71.53% reduction in PDP at 1.8V with respect to standard 6T SRAM and 9.89% reduction in power , 29.11% reduction in PDP at 1.8V with respect to existing 9T SRAM as shown in table-I.

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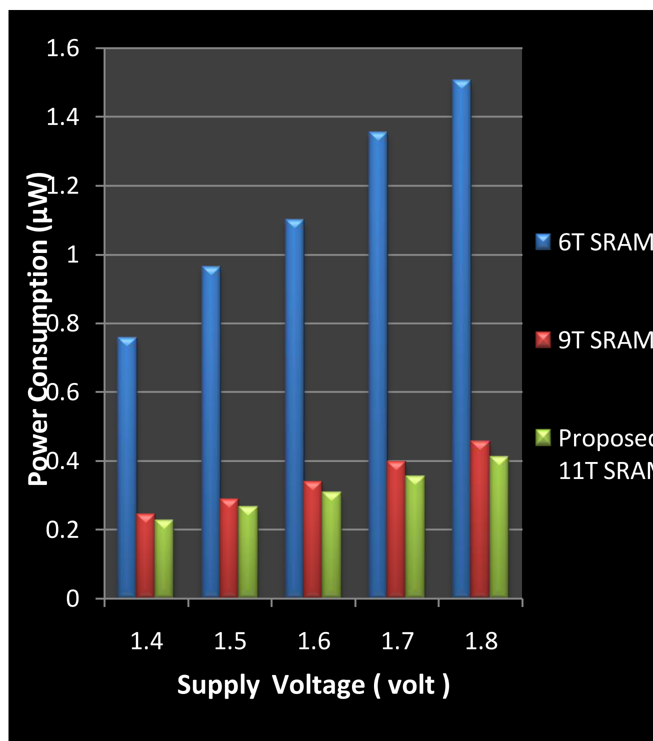
The significant improvement at other voltages can be analysed from the Table-II and Table-III. The proposed circuit has been mainly designed for bit-interleaving application with better performances compared to earlier design of 9T SRAM in term of power, speed and PDP.

Table 1 - Power consumption and Delay of existing and proposed SRAM cell at 1.8V.

SRAM CELL	Power(μW)	Delay(pS)	PDP (fWS)
6T SRAM	1.504	48.12	72.372
9T SRAM	0.455	63.88	29.065
Proposed 11T SRAM	0.410	50.25	20.602

Table 2- Power consumption and Delay of existing and proposed SRAM cell at 1.6V.

SRAM CELL	Power(μW)	Delay(pS)	PDP (fWS)
6T SRAM	1.099	55.19	60.653
9T SRAM	0.337	67.89	22.878
Proposed 11T SRAM	0.307	55.54	17.050



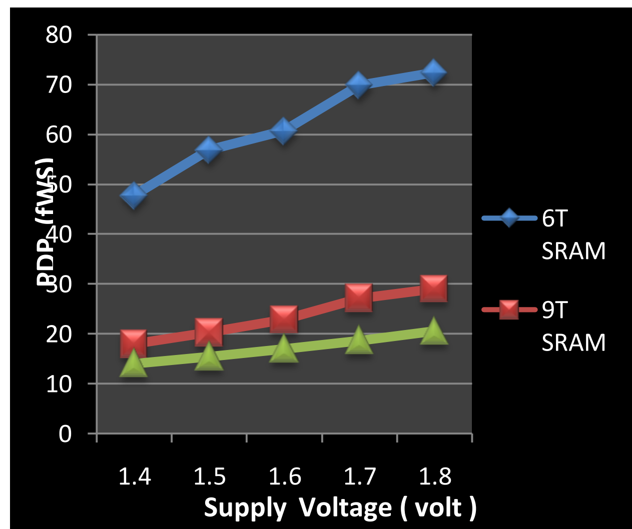


Fig.6. Variation of power and PDP with supply voltages.

2. Stability Analysis

The stability of SRAM cell is defined by static noise margin (SNM); the higher the SNM the better the stability. SNM is defining maximum DC noise voltage that can be tolerate by the cell without changing the output bit or stored bit. So the cell stability is depends on supply voltage, as supply voltage is reduce the cell become less stable.

The most common static approach for measuring the SNM is by using butterfly curves, which is obtain from a dc simulation. The SNM of the SRAM cell is defined as the size of the largest square that can fit into the butterfly curve [25].

The hold stability of the SRAM is defined by the HSNM (Hold SNM). In 9T and proposed 11T cell the butterfly curve appear asymmetrical due to the asymmetrical stored structure. Hence the HSNM equals to the smaller one of the two maximum squares. Butterfly curves for HSNM calculation is shown in Fig. 7.

SNM = min (SNM 1, SNM 2)

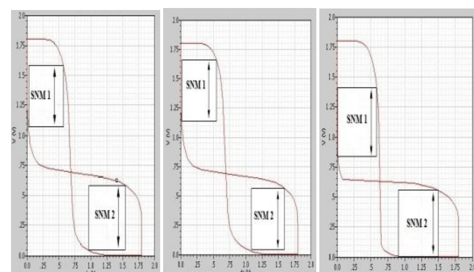


Fig.7. Statistical butterfly curves of Hold mode (a) 6T (b) 9T (c) Proposed 11T.

Table 3 - SNM of existing and proposed SRAM cell at 1.8V.

SRAM CELL	HSNM	WSNM	RSNM
6T SRAM	528 mV	460 mV	83 mV
9T SRAM	516 mV	533 mV	71 mV
Proposed 11T SRAM	558 mV	583 mV	107 mV

V. CONCLUSION

In this paper, a novel 11T SRAM cell with bit-interleaving capability has been proposed. The main motive of this paper is to reduce the power consumption, improve the stability of proposed design. Analysis of results show that, the proposed 11T SRAM cell is giving better performance in terms of stability, power consumption and PDP with respect to standard 6T SRAM cell and 9T SRAM with bit-interleaving capability. The delay of the circuit is increased slightly at the voltages above 1.6V in comparison with that of standard 6T SRAM cell but PDP of the circuit reduces in significant amount at all the voltages. While significant reduction in both delay and power consumption is observed with respect to 9T SRAM. Also the proposed circuit has bit-interleaving capability to reduce soft error probability.

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