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A Novel Sleep Switch leakage Mitigation technique in DSM Technology

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Abstract – **This paper proposes new technique ON OFF based domino and examines with inputs and clock signals combination in 32nm technology with footerless domino circuit for reduced leakage current. In this technique a p-type and an n-type pass transistor logic are introduced between the pull-up and pull-down network and the gate of one is controlled by the source of the other. Therefore the main focus in proposed work is given into the noise immunity of the circuit. The problem of leakage current here is optimally solved by the keeper transistor logic. In the proposed work two keeper transistor terminologies is taken into account which gives better performance in delay variability which is a big concern for high performance circuit application. The proposed circuit technique for AND2, OR2, OR4 and OR8 circuits reduces the active power consumption by 50.94% to 75.68% and by 64.85% to 86.57% at low and high die temperatures respectively when compared to the standard dual threshold voltage domino logic circuits.**

Keywords – **Leakage current; stacking; MTCMOS; dual threshold CMOS, ONOFIC.**

I. INTRODUCTION

Modern device dimensions have been scaled down since the last two decades and the number of transistors on a chip has thus increased to integrate more applications in a small area. Device miniaturization increases the device density on single silicon buffer and reduces the propagation delay. Switching speed of the CMOS circuit is inversely proportional to the delay of that logic circuit. Equation (1) shows that the threshold voltage of the device must be reduced proportionally by reducing the supply voltage of the device so that it should maintain the performance of the device. However, the main component of the leakage current called sub-threshold, increases exponentially when the threshold voltage of the device is reduced. Sub-threshold leakage current of the device.

All these above mentioned leakage currents come in to picture only in sub-micron technology. Reverse bias p-n junction leakage current in a MOS circuit is caused by the two main components. They are minority carrier diffusion process or drift process near the edge of depletion region of the p-n junction in MOS circuit and other is because of the electron-hole pair generation in depletion region when p-n junction is reverse bias. Sub-threshold leakage current in a MOS circuit occurs when weak inversion region is formed, which happens when gate voltage is below threshold voltage. It is present between source and drain in a MOS transistor for low gate voltages. In the weak inversion, the concentration of minority carrier in the channel of MOS is little, but not zeros, because of this reason sub-threshold leakage current flows, this leakage current one of the major reasons for leakage current. Gate oxide tunnelling leakage current is flowing form gate to substrate through the gate oxide due to tunnelling of electrons. If thickness of the gate oxide layer is reduced, then the electric field across the gate oxide increases. The high electric field across the low oxide thickness results in tunnelling of electrons form gate to substrate. Gate current due to hot-carrier injection flows only in a short-channel transistor because of the high electric field that is present near the Si-SiO_2 interface. So that electron and hole obtain enough amount of energy needed to cross the potential barrier and enter the gate oxide layer, this process is called hot-carrier injection. This energy is extracted from the high electric field. In the injection process electrons have a lower effective mass than hole and barrier potential for hole is more than barrier potential for electron. Gate-induced drain leakage current flows due to high electric field in the drain junction of the MOS transistor. When voltage is applied at the gate terminal of transistor accumulation happens at the silicon surface, the silicon surface has almost same potential as the p-type substrate. Holes are accumulated at the surface to form the accumulation layer, so the surface behaves like a p-region and heavily doped as compared to the substrate of the MOS transistor. Punch-through leakage current flows in short-channel devices only. Mainly there are two p-n junctions in transistors, in which the depletion layer at the drain and the source-substrate junction extends into the channel. In a short-channel device the channel length is small, if doping of the substrate is constant, then a space charge region exists in between the source to substrate junction and drain to substrate junction. If drain to source voltage increases than the reverse bias of the junction increases, so that depletion layer of the junctions also increases and at the same time the depletion layer of the junctions merge, and punch-through occurs and leakage current flows.

This paper proposes a novel leakage reduction technique that reduces leakage significantly without much overhead in power/area and performance. The simulation results shows that proposed approach of leakage reduction provides significant reduction in leakage current over the existing technique. Thus, proposed method of leakage reduction can be effectively utilized in portable devices.

II. SOURCES OF LEAKAGE AND DIFFERENT LEAKAGE REDUCTION TECHNIQUES

Significant efforts have been devoted to reduce leakage. Before getting detailed discussion on the different leakage reduction techniques, the first subsection shows different sources of leakage in theVLSI chips.

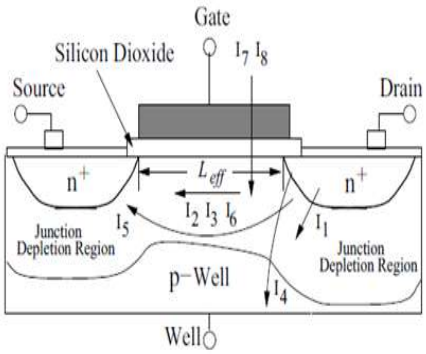

Fig.1. Leakage Mechanism in Short-Channel NMOS Transistor

2.1 Sources of Leakage:

The static power dissipation can be calculated by the product of the leakage current flowing in the device and the supply voltage:

$$P_s = i_{leakage} * V_{dd}$$

There are six major sources of leakage in the sub-nanometer MOS device as shown in Figure 1. Figure1: Sources of leakage in a transistor From the figure it can be seen that I1 is the reverse bias pn-junction leakage current whereas I2 is the sub-threshold leakage. It is current drain-to-source current flows while the gate is biased below threshold voltage. I3 is the oxide tunneling current which arises
due to large electric field and can be overcome by considering high-K material. I4 represents leakage due to hot carrier injection whereas I5 is gate induced drain leakage. Finally the I6 represent punch through current which is excessive and may burn out the transistor.

2.2 Leakage Reduction Techniques:

This section details different leakage reduction techniques.

2.2.1 Transistor Stacking [5]: The sub-threshold current in the transistor reduces significantly when
two or more transistor in series is in off condition. In this condition, source voltage of the stacked transistor increases that reduces, gate-to-source (VGS) voltage, drain-to-source (VDS) voltage and increases the body reverse biasing voltage (VBS) as shown in Figure 2. Figure 2: Illustration of ransistor stacking All these effects result in significant reduction in the leakage current. In order to further reduce the leakage, more number of the series connected transistors are applied the input that made them turned off. The approach is sometimes called as forced stack technique.

2.2.2 Dual Threshold
In this technique transistors which are in non-critical path are kept at higher threshold to reduce the leakage whereas the transistors in critical path fabricated with low threshold as shown in Figure 3. The lower threshold in the critical path reduces the delay of the design whereas higher threshold on non-critical path allows lower leakage of the circuit. Thus the dual threshold technique provides lower leakage without disturbing the performance of the design.
LECTOR Technique [7]:

The Leakage Control transisTOR (LECTOR) technique uses two leakage control transistors (LCTs) (a PMOS and an NMOS) in CMOS logic as shown in Figure 5. In this approach, each LCT transistor is controlled by the other LCT. Since one of the LCT is always near its cut-off for any combination of input signal, it decreases current in the path from VDD to ground. LECTOR is single threshold, an input pattern independent scheme which inserts two transistors in the path between pull-up and pull-down logic circuit. The concept of LECTOR technique is an application of transistors stack in the path from the power supply to ground. When one or more transistors are in cut-off mode then they behave as large value resistance and mitigate the leakage current. LECTOR is capable to reduce leakage current in both active and standby modes.

Fig.2. LECTOR based NOT Gate

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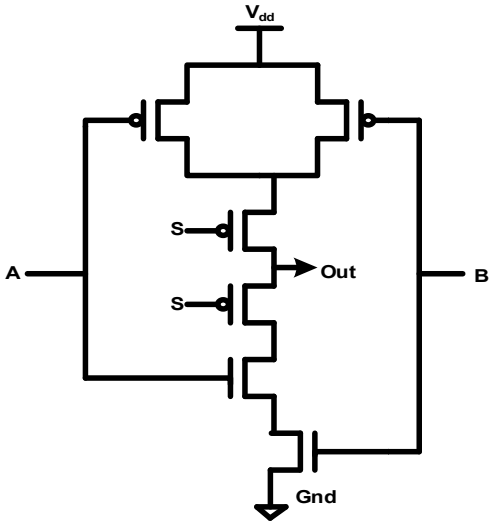
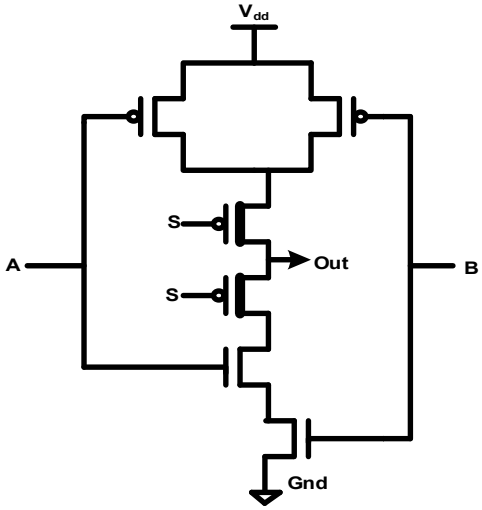
III. Proposed Circuit

In this section a novel designe are introduced namely modified ONOFIC approach with and sleep transistor at Header and Footer known as power gated technique. These are the combinations of self controlling and external leakage controlling technique. In self controlling technique no external signals are applied while in external leakage controlling technique external sleep signal are applied which switches OFF the sleep transistor to reduces the leakage power. The basic idea behind all the proposed techniques is to provide stacking effect of the transistor which mitigates leakage power from V_{dd} to GND as shown in Figure.3.



(a)



(b)Fig.3. (a) Proposed Sleep Switch Low V_{th} (b) Sleep Switch with high V_{th}

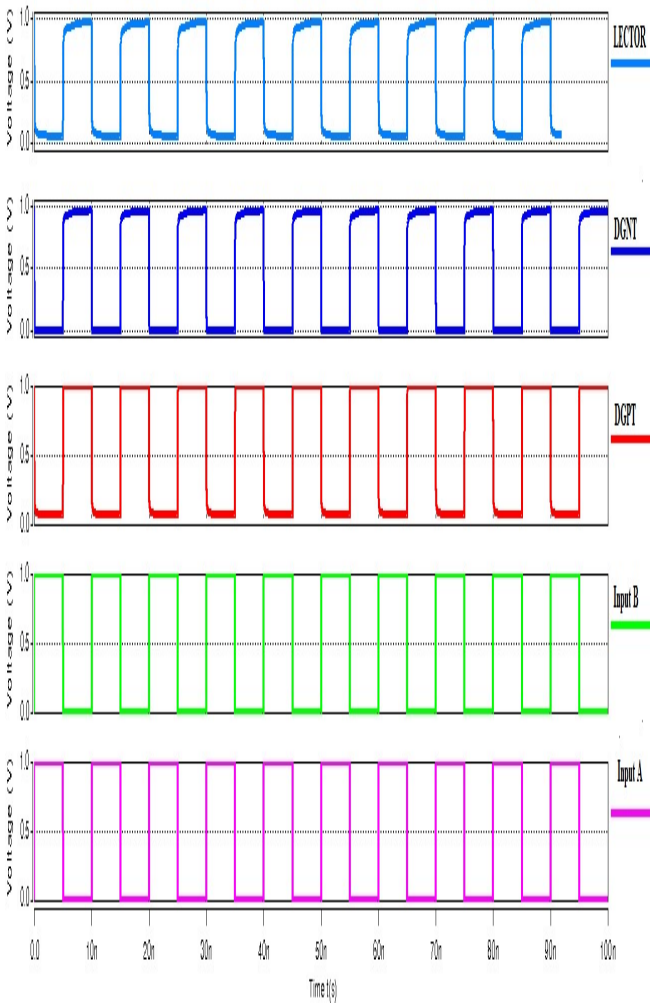


Fig. 4 Transient characteristics waveform of 2-input proposed Sleep Switch NAND gate using HSPICE in FinFET technology.

IV. RESULTS AND DISCUSSION

The existing and proposed techniques are simulated in CMOS at 32nm technology with supply voltage of 1V, output capacitance C_L=1pF, temperature 25^0C and 110^0C, W/L ratio is 4 for pull up and 2 for pull down network for all existing and proposed circuit. Similarly for leakage controlling transistor W/L ratio are same. This equal ratio is kept in order to make a fair comparison and identical rise and fall time of results. All the existing and proposed technique are simulated in SPICE at 32nm technology with supply voltage of 0.9V, output capacitance C_L =1pF, Leakage power is investigate at different temperature at 25^0C and 110^0C, The size (W/L) of all existing and proposed circuit made from P-MOS and N-MOS is same for fair comparison of results it is observed that leakage power has mitigated as shown in Table II, III, IV and V

Table.1. Calculation of Average Power, Delay, PDP and EDP at 32nm.

	Average Power (μW)	Delay (pS)	PDP(aS)	EDP(E-30)
Basic Inverter	3.263	24.45	79.78	1950
Basic NAND Gate	2.683	36.36	97.55	3546
Basic NOR Gate	2.432	15.72	38.23	600.9
LECTOR Inverter	2.354	44.36	104.4	4631
LECTOR NAND Gate	2.479	43.76	108.4	4743
LECTOR NOR Gate	2.225	33.85	75.31	2549
ON OFF Inverter	2.197	42.46	93.28	3960
ON OFF NAND Gate	2.583	45.24	116.8	5284
ON OFF NOR Gate	2.386	20.73	49.46	1025
Proposed Sleep Switch NAND Gate	1.029	31.25	32.15	1004

Table 2. Leakage Power Dissipation of Basic gates for two input vector

Gates	Temp	Leakage Power Dissipation (nW)							
		Low Vth				High Vth			
		[00]	**[01]**	**[10]**	**[11]**	**[00]**	**[01]**	**[10]**	**[11]**
NOT Gate	25^0C	7.868 (For 0 Input)	0.946 (For 1 Input)			1.641 (For 0 Input)	0.0569 (For 1 Input)		
	110^0C	95.61 (For0 Input)	36.59 (For 1 Input)			24.75 (For 0 Input)	3.873 (For 1 Input)		
NOR Gate	25^0C	15.72	0.943	0.837	0.531	3.280	0.056	0.047	0.002
	110^0C	190.4	34.13	34.04	3.375	49.36	3.806	3.331	0.312
AND Gate	25^0C	12.70	20.05	19.93	9.778	0.368	1.880	1.837	1.755
	110^0C	392.1	454.0	485.1	175.1	19.74	41.51	41.11	32.74
NAND Gate	25^0C	0.535	7.840	7.723	1.893	0.128	1.639	1.596	0.113
	110^0C	9.746	92.66	93.63	72.42	2.873	24.43	24.04	7.726
EXOR Gate	25^0C	15.55	1.816	1.816	15.55	3.233	0.104	0.104	3.233
	110^0C	185.6	67.77	67.77	185.6	48.34	7.124	7.124	48.34
EXNOR Gate	25^0C	15.67	1.886	1.746	15.44	3.276	0.113	0.094	3.190
	110^0C	184.5	67.66	67.88	186.6	48.72	7.588	6.660	47.96

Table 3. Leakage Power Dissipation in ON OFF approach in Basic gates for two input vector

Gates	Temp	Leakage Power Dissipation (nW)							
		Low Vth				High Vth			
		[00]	**[01]**	**[10]**	**[11]**	**[00]**	**[01]**	**[10]**	**[11]**
NOT Gate	25^0C	0.3077 (For 0 Input)	0.082 (For 1 Input)			0126 (For 0 Input)	0.0471 (For 1 Input)		
	110^0C	20.73 (For 0 Input)	6.271 (For 1 Input)			12.49 (For 0 Input)	3.292 (For 1 Input)		
NOR Gate	25^0C	13.43	0.8462	0.8329	0.0527	2.435	0.0470	0.0449	0.0027
	110^0C	163.0	30.37	31.66	3.329	39.32	3.245	3.162	0.3079
AND Gate	25^0C	0.8434	7.209	7.206	1.975	0.3781	5.252	5.189	0.8345
	110^0C	35.07	107.95	109.6	85.55	23.178	67.182	66.163	1.562
NAND Gate	25^0C	0.5231	6.887	6.884	1.659	0.1229	1.265	1.263	0.0911
	110^0C	9.609	82.32	84.06	61.99	2.794	20.38	20.45	6.335
EXOR Gate	25^0C	0.9282	0.3186	0.3186	0.9282	0.0897	0.2318	0.2318	0.0897
	110^0C	7.549	23.11	23.11	7.549	6.211	19.361	19.361	6.211
EXNOR Gate	25^0C	0.3168	0.0901	0.0901	0.3168	0.2481	0.0518	0.0518	0.2481
	110^0C	23.11	6.938	6.938	23.11	20.732	4.735	4.735	20.732

Table 4. Leakage Power Dissipation in Proposed Sleep Switch for two input vector

Gates	Temp	Leakage Power Dissipation (nW)							
		Low Vth				High Vth			
		[00]	**[01]**	**[10]**	**[11]**	**[00]**	**[01]**	**[10]**	**[11]**
NOT Gate	25^0C	0.051 (For 0 Input)	0.022 (For 1 Input)			0.0027 (For 0 Input)	0.0011 (For 1 Input)		
	110^0C	3.103 (For 0 Input)	1.568 (For 1 Input)			0.3031 (For 0 Input)	0.1413 (For 1 Input)		
NOR Gate	25^0C	0.052	0.022	0.022	0.014	0.0027	0.0011	0.0011	0.0072
	110^0C	3.211	1.562	1.565	0.999	0.3049	0.1415	0.1415	0.0894
AND Gate	25^0C	1080.9	1088.7	1088.7	874.1	91.25	91.28	91.28	98.211
	110^0C	2214.6	2421.1	2421.1	3114	113.14	119.96	119.96	167.66
NAND Gate	25^0C	0.040	0.051	0.051	0.031	0.0024	0.0027	0.0027	0.0019
	110^0C	1.560	3.100	3.103	2.104	0.2531	0.3036	0.3036	0.1806
EXOR Gate	25^0C	0.0310	0.0525	0.0525	0.031	0.0015	0.0027	0.0027	0.0017
	110^0C	2.100	3.211	3.211	2.100	0.1908	0.0015	0.3079	0.1718
EXNOR Gate	25^0C	0.0525	0.0310	0.0310	0.052	0.0027	0.0019	0.0015	0.0027
	110^0C	3.210	2.099	2.101	3.211	0.3079	0.1908	0.0019	0.3079

V. Conclusion

Leakage reduction solution as compared with the other conventional and relevant techniques and there is no need of technology modification, no change of fan-out logic state of WLS gates during idle mode and needs no additional power supply. Trade–off between area, delay and power requirements can be obtained by the use of specific variant in a given circuitAnd every variants suitable for specific performance parameter like V1, and V2 is better when speed is our main concern, it reduces 14.58% of the average delay for these circuits, but in this case W/L ration of PMOS must be adjust. Table.I and II shows overall optimum result for leakage reduction and power.

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