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A Review Article of Instrumentation Amplifier 16-Bit Pipelined Analog-to Digital Converter (Adc) Designed

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***Abstract* – An Instrumentation Amplifier 16-bit pipelined analog-to digital converter (ADC) is designed in this Report. The pipelined architecture realizes the high-speed and high-resolution. To reduce some complexities of flash ADC pipeline ADC is used. The calibration schemes of pipelined ADC limit absolute and relative accuracy. Deviations in residue amplifier gain results due to low intrinsic gain of transistors, and mismatching between all the capacitors of capacitance 1pF result in both deviations in residue amplifier gain and DAC nonlinearity in a pipelined ADC. To image the world, a low-power CMOS image sensor array is required in the vision processor. The image Instrumentation Amplifier array is typically formed through photo diodes and analog to digital converter (ADC). To achieve low power acquisition, a low-power mid-resolution ADC is necessary. Digital correction allows also to use very low power dynamic comparators. The multiplying D/A converters (MDACs) utilize a modified folded dynamic amplifier.**

***Keywords* – ADC, Pipelined, 16-bit, CLS, Fully differential, low power circuit design.**

I. INTRODUCTION

Over the last decade, much of the research on Instrumentation Amplifier analog-to-digital converters (ADC) has been focused on developing architectures such as pipelined [1] and sigma-delta converters [2], and pushing the limits of performance in resolution and speed. The work presented here focuses on moderate resolution, and moderate speed, but ultra-low-power ADCs. Such Instrumentation Amplifier ADCs will be critical in the emergence of large scale sensor networks.

Distributed sensors utilizing low-power sensor motes are becoming a popular solution for data gathering in hazardous environment. Integrated CMOS sensors with built-in data acquisition signal conditioning and transmission are needed for such applications. However, there is strict energy consumption limit for these sensors, since most of these sensors plan to use energy from scavenging the environment, or through a single battery to last a lifetime.

The ADC used in such sensors act as the crucial interface between the sensed environment and the sensor network as a whole. The network exploits the spatial redundancy of the sensors in any available location to obtain accurate sensor data. Hence resolution and accuracy of the ADC in a single sensor mote is not critical.

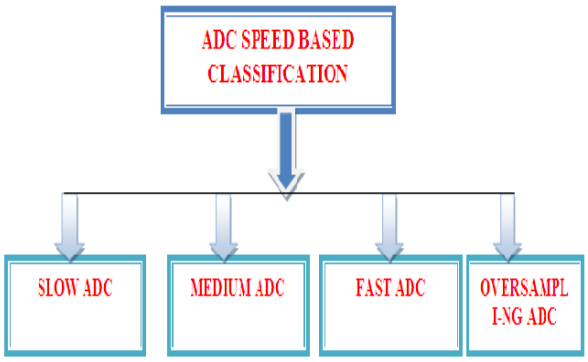

Fig.1.Different types of ADC

An autonomous node in a sensor network ideally contains a sensor, a readout circuit, a digital signal processing part to process information from the sensor and a Instrumentation Amplifier circuit.

The central base station which functions as a network controller collects the data from all the sensor nodes and extracts meaningful information of the target material by performing advanced digital signal processing. Fig.1. demonstrates the conceptual block diagram of distributed sensing using N redundant sensors.

As seen, the system has the front-end which converts the raw signal from the sensor to the electrical signal. At the

second stage, ADC converts the electrical signals into the digital signals which are much easier to process. The digital signals so received are converted into analog signal in order to be transmitted as the radio frequency signal through Power Amplifier.

II. LITRETURE SURVEY

James Lin, Member, IEEE, Daehwa Paik, and Seungjong Lee: This paper presents a 0.55 V, 7 bit, 160 MS/s pipeline ADC using dynamic amplifiers. In this ADC, high-speed open-loop dynamic amplifiers with a common-mode detection technique are used as residue amplifiers to increase the ADC's speed, to enhance the robustness against supply voltage scaling, and to realize clocks callable power consumption. To mitigate the absolute gain constraint of the residue amplifiers in a pipeline ADC, the interpolated pipeline architecture is employed to shift the gain requirement from absolute to relative accuracy. To show the new requirements of the residue amplifiers, the effects of gain mismatch and nonlinearity of the dynamic amplifiers are analyzed.

Ali Meaamar, Student Member IEEE,1Masuri Bin Othman: A fully differential, high gain opamp to be used in a low-voltage low-power high speed pipeline analog to digital converter (ADC) in a 0.18,um CMOS process is designed. The opamp architecture is based on folded cascade and "double differential amplifier" technique. This design operates of a 1.8V power supply, achieving a differential output swing of ±1.65V, a DC gain of > 95 dB with a unity gain at 312MHz and a phase margin of 560 and 0.5mW power dissipation.

Thomas Liechti, Armin Tajalli, Omer Can Akgun, Zeynep Toprak, and Yusuf Leblebici: This paper describes the implementation of a 12-bit 230 MS/s pipelined ADC using a conventional 1.8V, 0.18µm digital CMOS process. Two-stage folded cascode OTA topology is used for improved settling performance. Extreme low-skew (less than 3ps peak-to-peak) chip-level clock distribution is ensured by five-level balanced clock tree, implemented in low swing current-mode logic. The ADC block achieves a peak SFDR of 71.3 dB and 9.26 ENOB at 230 MS/s, with an input signal swing of 1.5Vpp. The measured peak SFDR at 200 MS/s is 78 dB, while the peak SNDR at 200 MS/s is 59.5 dB. The SFDR and SNDR performance exhibits very flat characteristics, maintaining higher than 53 dB SNDR at 230 MS/s and higher than 58 dB SNDR at 200 MS/s, from DC through Nyquist rate input frequencies.

III. INSTRUMENTATION AMPLIFIER ADC DESIGN PARAMETERS

1. Fundamental Parameters

Low-power Instrumentation Amplifier design begins with analyzing and understanding the fundamental limits that constrain the design of the particular circuit or system. For ADC design, these limits ultimately determine the total energy that must be consumed during a data conversion cycle for a given resolution and sampling rate. While it is generally impractical to actually design circuits and systems based on fundamental limits alone, a good understanding of these limits is critical to achieving an optimized design.

2. Quantization Noise

Quantization noise is present in all Instrumentation Amplifier ADCs, including "ideal" converters. Even a perfect ADC generates a quantized output from a continuous input signal. Thus, quantization noise limits the information content of the ADC output. While the input signal can assume any level within the conversion range and can even go beyond the allowed input range, the output is confined to a set of discrete output values.

The mere process of converting a continuous analog input signal to a discrete digital output code results in a loss of amplitude information about that input signal. The amount of amplitude information lost in the conversion process depends on the resolution (number of bits) of the ADC.

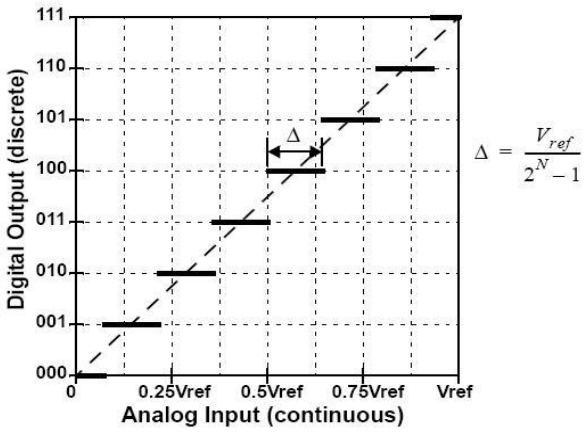

Fig.2. Transfer functions of an ideal 3-bit ADC. For an N-bit ADC there are 2N output levels corresponding to input voltage ranges of width Δ.

The output of the ideal Instrumentation Amplifier ADC depicted in Figure 3.1 is passed to an ideal digital-to-analog converter (DAC) so that the input signal is converted from the analog domain, into the digital domain, and then back again to the analog domain.

The resulting output of the DAC is not a replica of the original input signal even though both the ADC and DAC are ideal. Instead, due to the ADC quantization, the output contains an input signal dependent error. Figure 2.2 shows the resulting error of the DAC output as a function of the

ADC input. Note that this error due only to the ADC and is called the quantization error of the ADC [5].

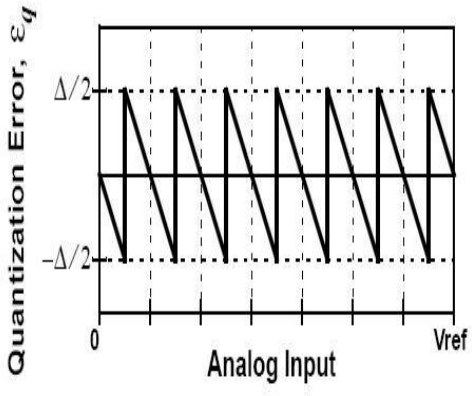

Fig.3 Error at the DAC output (from an ideal ADC-DAC series connection). The error comes purely from the quantization error of the ideal 3-bit ADC**.**

It is clear from Figure 3.2 that the quantization error as a function of time is determined by the input signal time domain behavior. While the quantization error signal can be calculated if the input signal is known this is useless since there is no need for an ADC at all if the input signal is known.

Thus it can be concluded that some amount of quantization error exists for all real input signals, but it is not possible to know the exact characteristics of the quantization error.

3. Proposed Frequency Scheduling Method

An adaptive method to perform dynamic voltage and frequency scheduling (DVFS) for minimizing the energy consumption of device chips is presented. Instead of using fixed update interval, the proposed DVFS system makes use of adaptive update intervals for optimal frequency and voltage scheduling. The system is interconnected with lead acid battery, the battery is connected to the Analog to Digital Converter (ADC) and it converts analytical electrical power to digital frequency.

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The battery is connected to the ADC and it converts analytical electrical power to digital frequency. Then the device is internally connected to the oscillator and the oscillator maintains the operating frequency level in that controller. Thus the converted digital frequency is send to the device. the controller detects the battery power level. If the battery power value is low, the operating frequency level In the device can be reduced by an oscillator.

The optimization enables the system to rapidly track the workload changes so as to meet soft real-time deadlines. The technique, which can be realized with very simple hardware, is completely transparent to the application. The results of applying the method to some real application workloads demonstrate considerable power savings and fewer frequency updates compared to DVFS systems based on fixed update intervals.

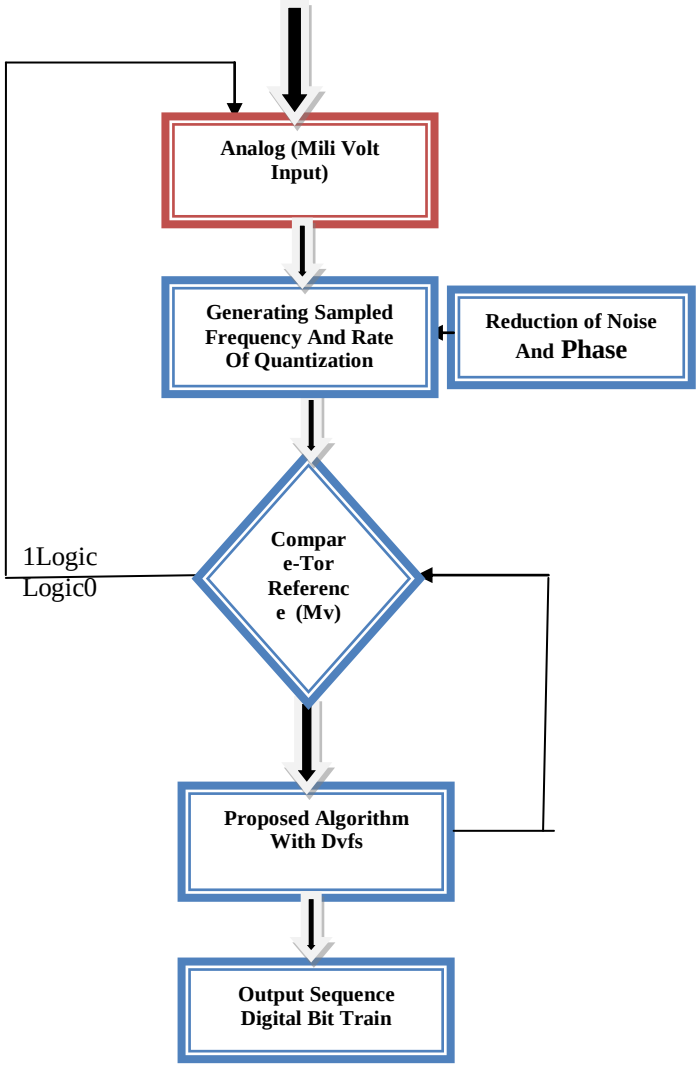

Fig.4. Proposed Algorithms Flow Chart.

IV. EXPECTED RESULT AND COMPARISION OF OLD METHODES

Instrumentation Amplifier Oversampled converters such as sigma-delta converters are potentially viable for this application. Sigma-delta ADCs can be made to be low-power [5] for a given resolution and sampling rate, however they are complex–requiring sophisticated clocking and filtering. In addition, the oversampled clock

needs to be much faster than the desired sampling rate. Generating the oversampled clock on each sensor node would likely offset any energy savings achieved in the rest of the ADC.

Table 5.1 Summary of performances of low-power ADCs

Architecture	Technology	Supply Voltage	Sampling Rate	Power (mW)
Delta-Sigma [32]	0.35-µm CMOS	1.8 V	1.4 MS/s	108
Successive Approximation [30]	0.25-µm CMOS	1V	100 KS/s	3.1
Successive Approximation [31]	0.18-µm CMOS	1 V	150 KS/s	30
Integrating [33]	1-µm CMOS	3.3 V	-----	-----
Algorithmic [34]	AMS BiCMOS 0.8-BYQ	2.8 V	2.9 KS/s	8.18 + 9.71
		2 V	0.7 KS/s	1 + 1.3

Continuing the survey of common architectures, integrating (single and dual slope) converters [5] possess many of the desired architectural features. They require very little analog circuitry, making them very low-power. Another disadvantage is that the conversion speed is very slow, in addition to the fact that the conversion period varies with input signal. The variable conversion period complicates the overall system design for the sensor node as a whole as different ADC samples will take different amounts of time.

V. CONCLUSION

This enables the use of dynamic amplifiers in a pipeline ADC. In addition, the dynamic amplifier offers both clock scalability and high-speed operation even with a scaled supply voltage. Using the above techniques, a 16 bit prototype ADC achieves a conversion rate of 160 MS/s with a supply voltage of 0.55 V. Therefore, the combination of interpolated pipeline architecture and dynamic residue amplifiers demonstrates the feasibility of ultra-low voltage high-speed analog circuit design. To implement the whole system a low-power and small size capacitance value sensing readout circuit is required. Also, it has to be integrated together with the back-end low-power current-mode ADC on the same chip. The low-power current-mode ADC has been designed and fabricated with TSMC 0.18um CMOS technology. In the simulation result, the power consumption for 16-bit ADC was 6 W, with a power supply of 0.65 V.The targeted specifications are met with the simulations in the schematic level and it has been shown that power consumption of the ADC using correlated level shifting is low.

VI. FUTURE WORK

The entire design has to be laid out and will be fabricated in IBM 130nm process. At the time of this documentation, the layout for the schematics has been started and will be used in the Large Harden Collider once the chip is taped out. There are two possible areas of improvement in this design:

- One possible improvement that could be realized for this design is on the fine settling amplifier. The bandwidth of this amplifier can be increased and as a result the speed of ADC can be improved. The ADC is operating up to 30MHz and with the improvement it is expected to work up to 40MHz;

- Another improvement that could be realized is to use a lower specification amplifier for last three 2.5bit stages as they do not require the higher specification power hungry amplifiers used in the first three stages. This could result in the further reduction of power and hence result in increase of ADC's figure of merit.

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