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Enhancement of Soft Core Processor Clock Synchronization DDR Controller and SDRAM by Using RISC Architecture

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Abstract – **With the ongoing advancements in the present VLSI industry System-on-Chip (SoC) is allowed to integrate multiple complex functions into a single chip, but still demand a single and shared main off-chip SDRAM for data storage. Consequently, the main memory controller has become an important factor in determining the overall system performance. It is a tough job to choose a memory controller that meets the exact demands of the whole system design. The Single Data Rate (SDR) SDRAM controller is to receive read and write requests, to generate the proper commands and to control the data bus of SDRAM. A 32-bit length Linear Feedback Shift Register (LFSR) is generates random number patterns automatically and those patterns are fed to the SDRAM and stored in it. The core controller then performs read/write operations to access the data stored in the memory banks. The core also performs all initialization and refresh functions. In this paper, we emphasized the designing of SDRAM controller architecture and its Interfacing with LFSR and SDR SDRAM. The design is described using VHDL language and simulations, resource utilization and power analysis are done in Xilinx ISE 14.5 and Modelsim 10.1b.**

Keywords – SDR SDRAM, Controller, LFSR.

I. INTRODUCTION

A processor is something which processes the given task. It is developed to make human task easy, and when it processes micro things it is called as a microprocessor. It contains basically two things. One is the CPU and second is the memory .CPU stands for central processing unit [1]. It controls the whole processor; we can also call it a human brain. The design of processor needs the designing of CPU and memory. The memory can be static or random. Design of CPU can be done in different ways but its fundamental operation remains the same. CPU is designed on small scale and large scale integration. Processors are designed with enhancements like decreasing power consumption, increasing more pipeline stages, increasing speed and minimizing the chip area. The basic operation performed by a processor is fetching, decoding and executing the given instruction. After that the output will store in memory. For storing the results in memory some mechanism is applied.

DDR Controller and Memory

With the rapid development in the processor's family, speed and capacity of a memory device is a major concern. The DDR is an enhancement to the traditional synchronous DRAM. The DDR is able to transfer the data on both the edges of each clock cycle. The DDR Controller mainly consists of four functional blocks:

- Address Latch
- Data Path
- Controller
- Counter

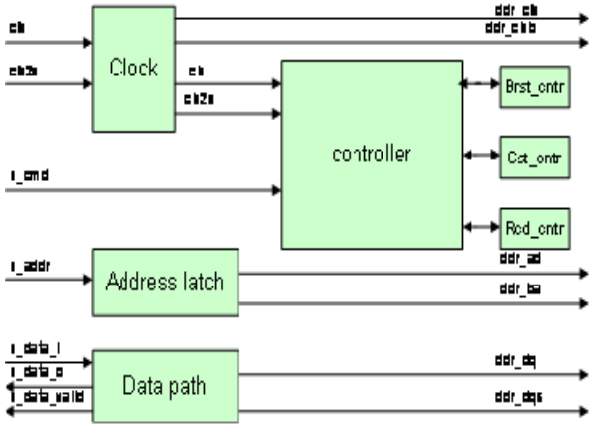

Fig 1 DDR Controller Architecture.

II. DIFFERENT FUNCTIONAL BLOCKS

1 Address Latch

The basic function of address latch module is to gets its control signals from the controller and generates row, column and bank addresses for the DDR SDRAM. The address latch also generates different control signals like burst_max, cas_lat_max for the burst counter and cas latency counter.

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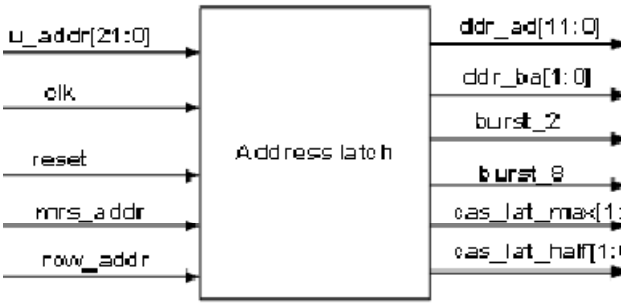

Fig. 2 Address Latch Module

2 Data Path

One of the most difficult aspects of DDR SDRAM controller design is to transmit and capture data at double data rate. This module transmits data to the memories. The basic function of data path module is storing the write data and calculates the value for read data path. Data path module handles all the data generation and sampling task of DDR controller. For Read access, data is sampled by data path. Data is then synchronized with the internal clock and transferred to the user interface one-word per clock cycle as normal data rate. For Write access, data is received from the user interface at the normal one word per clock data rate. The DDR controller's data path then resynchronized the data and transfers them using the double data rate.

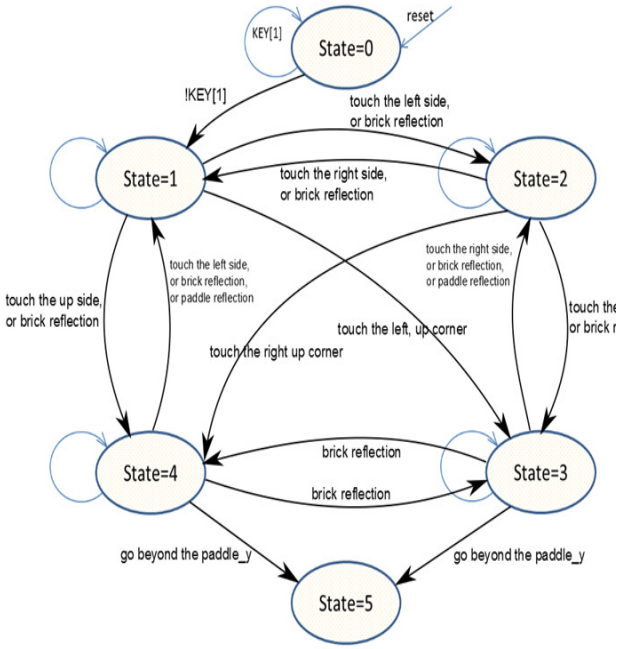

Fig. 3 State diagram.

3. Processor state machine diagram

Initially the controller is in the IDLE state. That means no operation is performing. A PRECHARGE ALL command is then applied. This command is used to deactivate any open row in a bank or the open bank row in all banks. Once a bank is pre charged, it is in idle state and must be activated prior to any READ and WRITE operation. Next a LOAD MODE REGISTER command should be issued for the extended mode register to enable the DLL, then another LOAD MODE REGISTER command to the mode register to reset the DLL and to program the operating parameters. Again a PRECHARGE command should be applied which place the device in all banks in IDLE state. In the IDLE state two AUTO REFRESH cycles must be performed.

4. Double Data Rate Source-synchronous Interfaces:

Double Data Rate (DDR) interfaces are becoming increasingly common in the ASIC world. A DDR interface is a type of source-synchronous interface meaning that the clock is sent along with the data from the transmitting device.

With traditional interfaces data will switch value either at rising edge or falling edge of the clock but not at both, this is called single data rate (SDR) and the data lasts for one full clock cycle. DDR interfaces allow data to be transferred at both rising edge and falling edge, thus providing twice the bandwidth of a SDR interface. Since data is transferred at both rising and falling edge the data only lasts for one half of a clock cycle, therefore DDR interfaces demands stricter timing requirements compared to SDR interfaces using the same clock frequency.

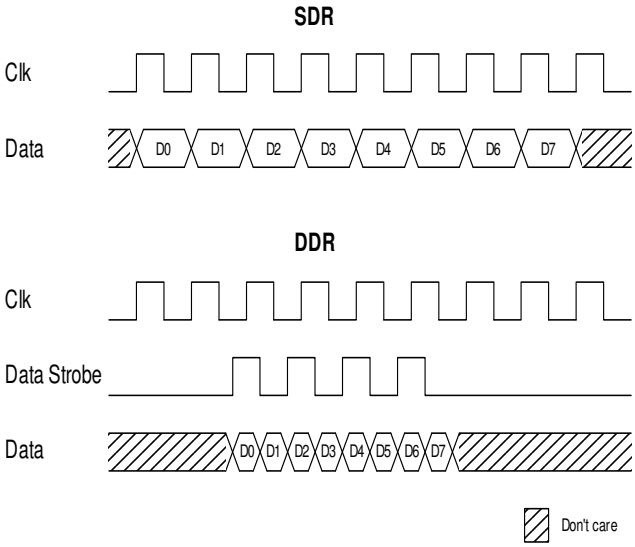

Fig. 4 Comparison of an eight beat burst with SDR and DDR.

The data strobe give a number of benefits compared to using a standard synchronous interface **Error! Reference source not found.**. A standard synchronous interface is limited to a time of flight between to ICs of one clock period while a source-synchronous interface has no time

of flight limits. A standard synchronous interface also has to deal with clock skews between the transceiver and receiver ICs but since a source-synchronous interface transmits the data strobe together with the transmitted data there is no skew. With a source-synchronous interface there is a synchronization challenge when communicating on the same bus with more than one IC. Every IC will transmit its own data strobe and data strobes from different ICs do not have to be in synchronization with each other. The receiving IC has to be able to sample data using the different data strobes making it challenging to design a resynchronization input buffer. The resynchronization buffer is used for sampling the data bus and synchronizes the data to the internal clock of the transceiver.

5. DDR SDRAM

As with standard SDRAM the architecture is pipelined and consists of multiple banks allowing concurrent operation and thereby providing high effective bandwidth **Error! Reference source not found.**, **Error! Reference source not found.** and **Error! Reference source not found.**. All reads and writes are burst oriented and are programmable to burst lengths of 2, 4 or 8 beats (other vendor specific burst lengths might exist).

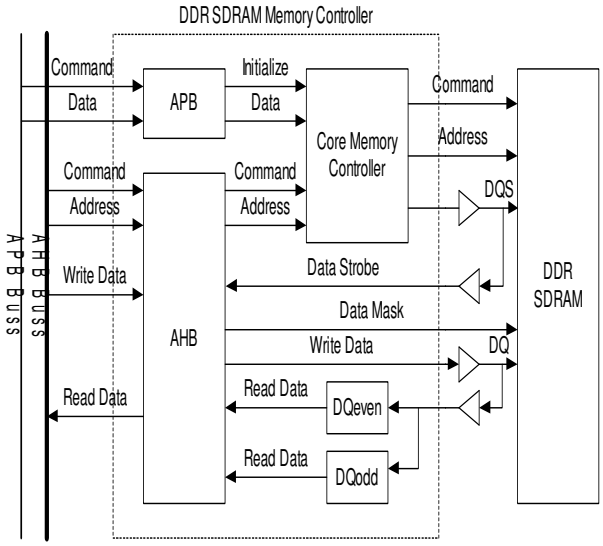

Fig. 5 Schematic view of the memory controller with one AHB Interface.

A DDR SDRAM is divided into four banks where each bank consists of a number of rows. A row is then divided into columns which each contains 32 bits of data. The number of rows and columns are dependent on the size of the DDR SDRAM and the internal organization. The organization with four banks makes it possible to issue one command to every bank. It is not possible though to make more than one read or write operation at a single time since the data bus only can handle data for one operation. It is possible to while a read or write burst is in progress in one bank to recharge and activate a row in one of the other banks.

6. DDR SDRAM Controller

The DDR SDRAM Controller (referred to as the memory controller) is designed to be able to support a various number of AHB slave interfaces. To achieve this, the control path and data path has been separated. The core memory controller handles the control path and the data path is incorporated into each AHB interface of the memory controller. An internal arbitrator decides which AHB interface that has access to the data path and the core memory controller. For the initialization of the memory controller there is also an APB interface. Through the APB interface EMRS and MRS registers are set up as well as the size and organization of the DDR SDRAM being used. The memory controller can handle a various number of DDR SDRAM chips and the maximum number of supported chips are decided upon synthesis.

When an AHB interface has been granted access to the data bus and the core memory controller the AHB interface can tell the core memory controller to do either a read or write operation. The AHB interface also tells how long the burst is going to be. The core memory controller then handles the activation of rows and if necessary splits the burst into more than one command and issues them to the DDR SDRAM. The core memory controller then signals to the AHB interface when data has to be sampled from or presented on the data bus depending on if it is a read or write operation that have been requested. The core memory controller handles all the timings that are involved when a command can or has to be issued to the DDR SDRAM.

III. SIMULATION AND RESULTS

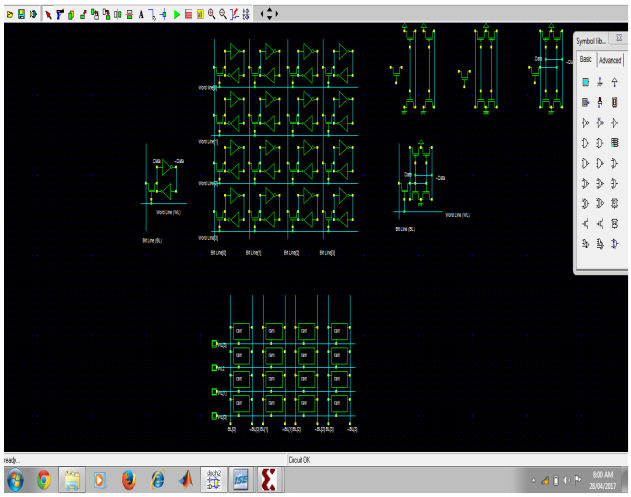

Fig. 6 Timing of SRAM design.

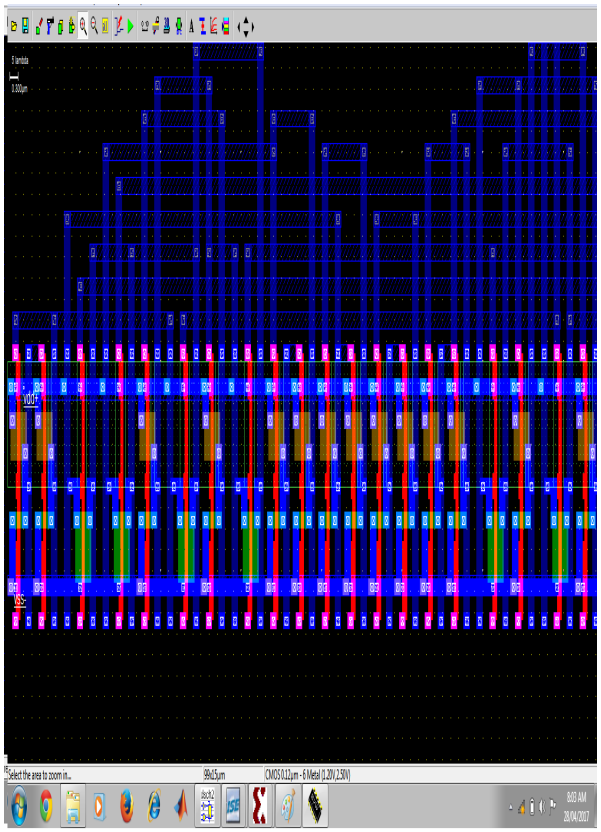

Fig. 7 Timing SDRAM LAYOUT design.

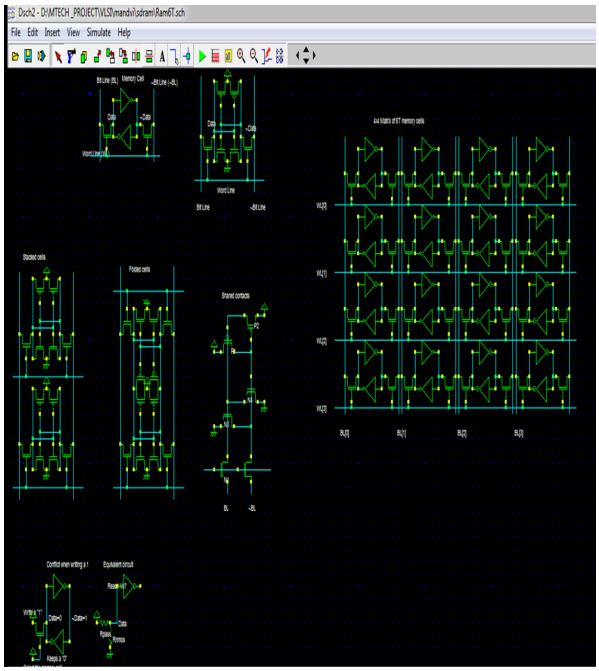

Fig. 8 Multi DDR SDRAM design.

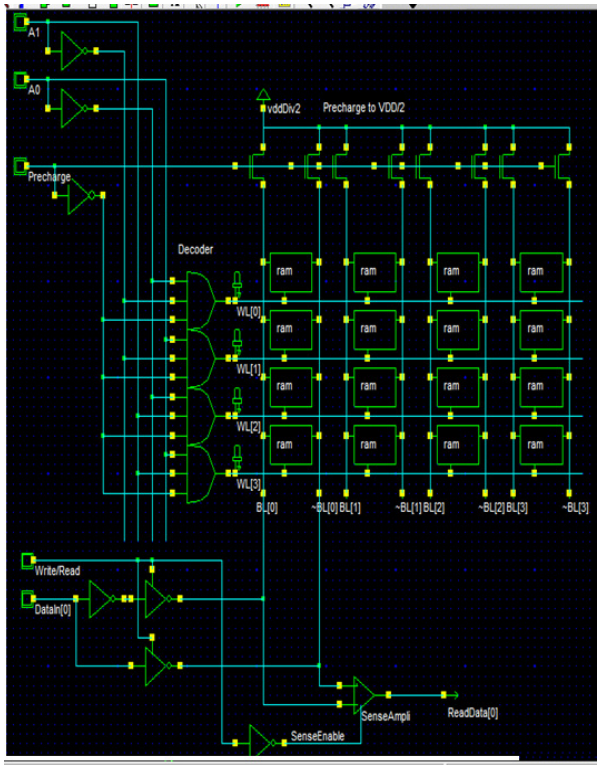

Fig. 9 16 Sense Schematic design.

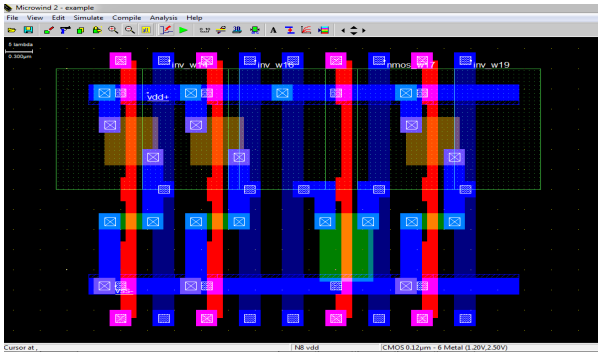

Fig. 10 Layout design 16 sense.

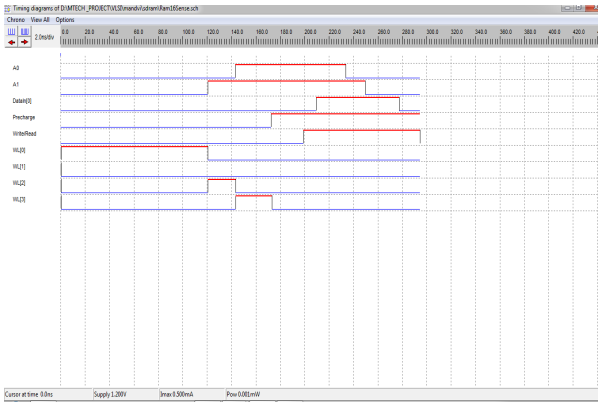

Fig. 11 Timing waveform16 sense.

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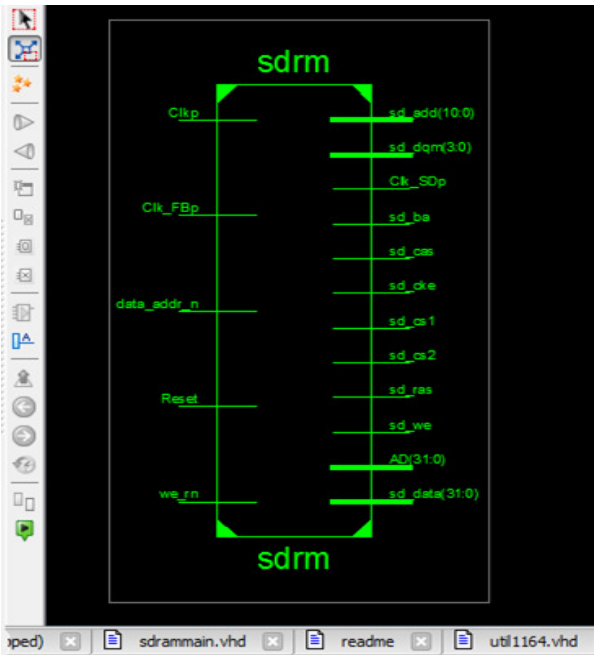

Fig. 12 SDRAM Xillinx Design.

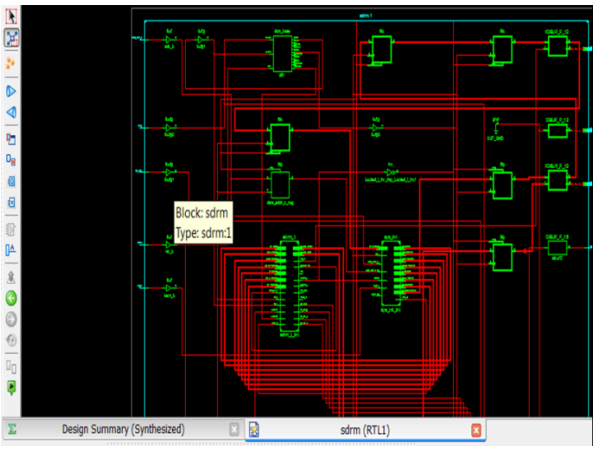

Fig. 13 RTL logic design.

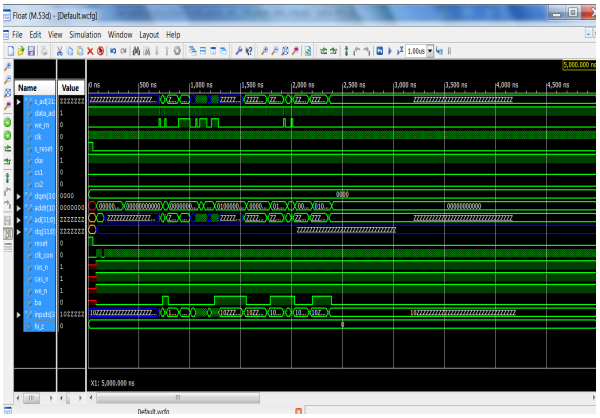

Fig. 14 Timing Waveform.

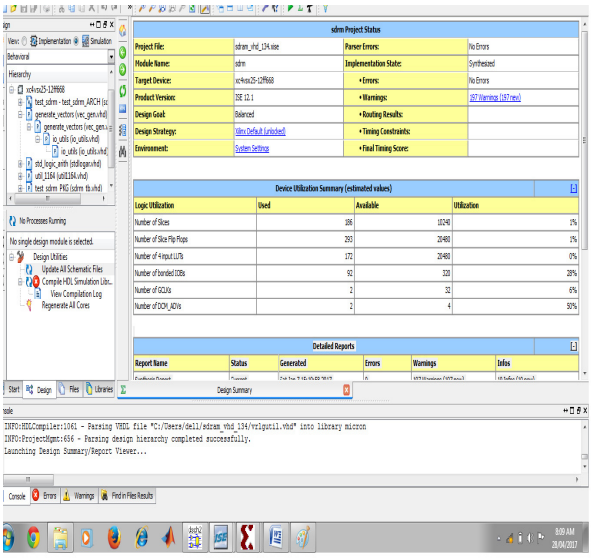

Fig. 15 Enhancement report.

IV. ENHANCEMENT REPORT

Macro Statistics:
 # Adders/Subtractors : 2 ,2-bit subtractor : 1,5-bit subtractor : 1
 # Counters : 4,14-bit down counter : 1,3-bit down counter : 1
4-bit down counter: 1,8-bit down counter : 1,# Registers : 66
1-bit register: 46,13-bit register : 5,16-bit register : 3
2-bit register: 4,3-bit register : 3,32-bit register : 3
5-bit register: 1,6-bit register : 1
 # Comparators: 3
3-bit comparator greater: 1,4-bit comparator greater : 1,8-bit comparator greater : 1
 # Tristates : 18
1-bit tristate buffer : 18
 # Registers: 249
Flip-Flops : 249
 # Shift Registers: 35
2-bit shift register: 32, 3-bit shift register: 2, 5-bit shift register: 1

OLD result in base paper Device utilization summary:
Selected Device: 3s50pq208-5
Number of Slices: 210 out of 768 27%
Number of Slice Flip Flops: 304 out of 1536 19%
Number of 4 input LUTs: 263 out of 1536 17% Number used as logic: 228
Number used as Shift registers: 35
Number of IOs: 146
Number of GCLKs: 3 out of 8 37%
Number of DCMs: 2 out of 2 100%
The design study shows that high-performance and large lookup table circuits can be implemented using low-cost

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state-of-the-art Processor and DDR3 technology. The proposed DDR3 SDRAM Controller design has been verified by the exhaustive functional verification. We examined the performance of the design by generating several test cases and noting down the time taken by the designed DDR3 Controller in finishing them. In most of the scenario the throughput of the design was close to the theoretical maximum.

V. CONCLUSION AND FUTURE WORK

Conventional 6T SRAM and MESFET 6T SRAM are analyzed through cadence virtuoso tool in 45 nm technology. It is seen that sub-threshold and gate leakage, both effects the operation of the SRAM cell. In this paper MESFET is used to simulate the 6T SRAM cell and it is concluded that MESFET increases the performance of SRAM cell. The considerable change in the sub-threshold leakage is observed in comparison with the gate leakage. Total leakage in the SRAM cell can be reduced to 10 % using MESFET. Further SVL technique is applied in MESFET SRAM cell in which LSVL provides increased ground voltage and USVL provides reduced supply voltage during standby mode which reduces the leakage by 34 %. Therefore, results in reduced power dissipation and increased performance.

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