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A Implementation of High Speed On-Chip Monitoring Circuit By Using SAR Based ADC Design

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Abstract – **An 16-bit pipelined analog-to digital converter (ADC) is designed in this thesis. The pipelined architecture realizes the high-speed and high-resolution. To reduce some complexities of flash ADC pipeline ADC is used. The calibration schemes of pipelined ADC limit absolute and relative accuracy. Deviations in residue amplifier gain results due to low intrinsic gain of transistors, and mismatching between all the capacitors of capacitance 1pF result in both deviations in residue amplifier gain and DAC nonlinearity in a pipelined ADC. To image the world, a low-power CMOS image sensor array is required in the vision processor. The image sensor array is typically formed through photo diodes and analog to digital converter (ADC). To achieve low power acquisition, a low-power mid-resolution ADC is necessary. Digital correction allows also to use very low power dynamic comparators. The multiplying D/A converters (MDACs) utilize a modified folded dynamic amplifier .In this enables to the use of dynamic amplifiers in a pipeline ADC. In addition, the dynamic amplifier offers both clock scalability and high-speed operation even with a scaled supply voltage. Using the above techniques, a 16 bit prototype ADC achieves a conversion rate of 160 MS/s with a supply voltage of 0.55 V. Therefore, the combination of interpolated pipeline architecture and dynamic residue amplifiers demonstrates the feasibility of ultra-low voltage high-speed analog circuit design. To implement the whole system a low-power and small size capacitance value sensing readout circuit is required. Also, it has to be integrated together with the back-end low-power current-mode ADC on the same chip. The low-power current-mode ADC has been designed and fabricated with TSMC 0.18um CMOS technology. In the simulation result, the power consumption for 6-bit ADC was 6 W, with a power supply of 0.65 V.**

Keywords – **Analog digital converter (ADC), CMOS circuits.**

I. Overview

Over the last decade, much of the research on analog-to-digital converters (ADC) has been focused on developing architectures such as pipelined [1] and sigma-delta converters [2], and pushing the limits of performance in resolution and speed. The work presented here focuses on moderate resolution, and moderate speed, but ultra-low-power ADCs. Such ADCs will be critical in the emergence of large scale sensor networks. Distributed sensors utilizing low-power sensor motes are becoming a popular solution for data gathering in hazardous environment. Integrated CMOS sensors with built-in data acquisition signal conditioning and transmission are needed for such applications. However, there is strict energy consumption limit for these sensors, since most of these sensors plan to use energy from scavenging the environment, or through a single battery to last a lifetime.

The ADC used in such sensors act as the crucial interface between the sensed environment and the sensor network as a whole. The network exploits the spatial redundancy of the sensors in any available location to obtain accurate sensor data. Hence resolution and accuracy of the ADC in a single sensor mote is not critical. . However, due to strict power budget, there is a stringent requirement on its energy consumption and area. Leveraging both CMOS device scaling and MEMS technologies, each mote will

integrate sensing, computation, communications and power into a volume on the order of 1 mm^3. The list of potential applications is tremendous, ranging from smart building environments, tracking wildlife populations, monitoring crops and livestock, and measuring and predicting weather patterns.

II. LITERATURE SURVEY

James Lin, Member, IEEE, Daehwa Paik, Seungjong Lee: This paper presents a 0.55 V, 7 bit, 160 MS/s pipeline ADC using dynamic amplifiers. In this ADC, high-speed open-loop dynamic amplifiers with a common-mode detection technique are used as residue amplifiers to increase the ADC's speed, to enhance the robustness against supply voltage scaling, and to realize clocks callable power consumption. To mitigate the absolute gain constraint of the residue amplifiers in a pipeline ADC, the interpolated pipeline architecture is employed to shift the gain requirement from absolute to relative accuracy.

Ali Meaamar, Student Member IEEE,1Masuri Bin Othman: A fully differential, high gain opamp to be used in a low-voltage low-power high speed pipeline analog to digital converter (ADC) in a 0.18,um CMOS process is designed. The opamp architecture is based on folded cascade and "double differential amplifier" technique. This design operates of a 1.8V power supply, achieving a differential output swing of ±1.65V, a DC gain of > 95 dB with a unity gain at 312MHz and a phase margin of 560 and 0.5mW power dissipation. The operational trans conductance amplifier (OTA) can be used to design high-speed ADCs, for local wireless communications.

Thomas Liechti, Armin Tajalli, Omer Can Akgun, ZeynepToprak, and Yusuf Leblebici: This paper describes the implementation of a 12-bit 230 MS/s pipelined ADC using a conventional 1.8V, 0.18µm digital CMOS process. Two-stage folded cascode OTA topology is used for improved settling performance. Extreme low-skew (less than 3ps peak-to-peak) chip-level clock distribution is ensured by five-level balanced clock tree, implemented in low swing current-mode logic.

Chun C. Lee, Member, IEEE, and Michael P. Flynn, Senior Member, IEEE: Successive approximation register (SAR) ADC architectures are popular for achieving high energy efficiency but they suffer from resolution and speed limitations. On the other hand pipeline ADC architectures can achieve high resolution and speed but have lower energy-efficiency and are more complex. We propose two stage pipeline ADC architecture with a large first stage resolution, enabled with the help of a SAR-based sub-ADC. The prototype12b50MS/s ADC achieves an ENO Bof10.4batNyquist and a figure-of-merit of 52 fJ /conversion-step.

III. ADC Architecture

When designing ultra-low-power circuits, energy considerations drive the design process from the choice of architecture all the way to the actual circuit Implementation. Choosing architecture is a critical point in the design process for such systems. A proper choice of architecture can lead to dramatic energy savings compared with alternatives. Conversely, a poor architectural decision can result in a sub-optimal design regardless of how well the individual circuit blocks are designed. While energy consumption is paramount in this application space, there are many other considerations driving the choice of ADC architecture. Figure 1 groups various ADC architectures that vary roughly by their achievable resolution, speed and power consumption [1]. Since low-power consumption is the primary design goal, Figure 5.1 shows that much architecture is poor choices. Time interleaved ADCs require multiple sets of analog hardware, leading to high power consumption but very fast sampling rates [2]. Flash converters [3] use a large number of comparators

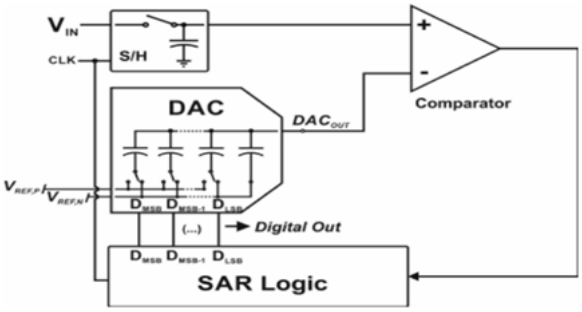


Fig. 1 ADC Architectures.

for a given resolution, making them impractical in most applications requiring more than 8 bits of resolution. Folding and/or interpolation [4] can help reduce the number of comparators required, but the architecture is still not well suited for low-power applications. Multi-step [5] ADC also require a relatively large amount of analog hardware, resulting in 25 excessive power consumption for application in distributed sensor networks. Some of the other ADC architectures, such as Delta-Sigma, Successive Approximation, Integrating and Algorithmic, have been reported to work with low-power consumption, low supply voltage and with moderate resolution and speed [3]-[2]. Some of the already existing low–power architectures are reviewed.

1. Delta- Sigma ADC

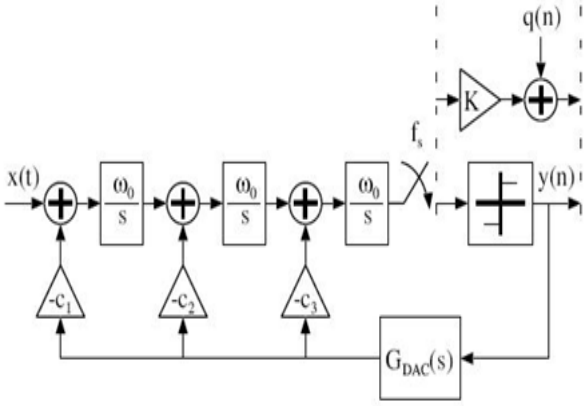


Figure 2 Continuous-time 3rd order Σ Δ-modulator block diagram [3].

Fig 2 shows the block diagram of a third order low-pass Σ Δ ADC employing a continuous time loop filter. The ADC [6] was reported to have a resolution of 10 bits and a dynamic range (DR) of 67 dB at a sampling rate of *f*s = 1.4MHz, while drawing a bias current of 60 μA from a modest supply voltage of 1.8V, thus consuming 108 μW of power. The ADC was designed in a 0.35-μm CMOS technology.

2. Successive Approximation

Shown in Fig 3, the successive approximation architecture uses only one comparator, along with simple digital logic and a switching network to implement the search algorithm. The ADC [3] was designed in a 0.25 μm CMOS process and was reported to consume 31pJ/8-bit sample at 1-V supply and 100 KS/s.

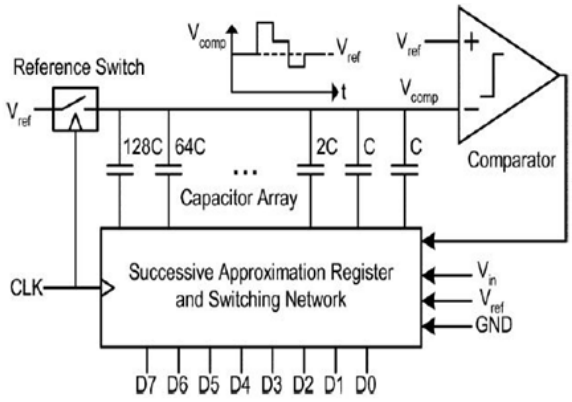


Fig. 3 Successive approximation architecture (shown for an 8-bit converter) [3]

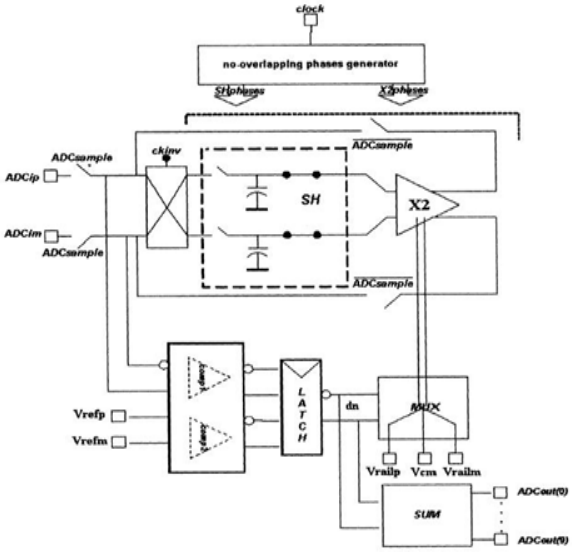


Fig. 4 Algorithmic ADC schematic Diagram [4].

The features of all the ADCs are summarized in the Table 2.

Table 1 Summary of performances of low-power ADCs.

Architecture	Technology	Supply voltage	Sampling Rate	Power (mW)
Delta-Sigma [2]	0.35-μm CMOS	1.8 V	1.4 MS/s	108
Successive Approximation [3]	0.25-μm CMOS	1V	100 KS/s	3.1
Successive Approximation [3]	0.18-μm CMOS	1 V-0.5 V	150 KS/s-4.1 KS/s	30-0.85
Integrating [3]	1-μm CMOS	3.3 V	-----	-----
Algorithmic [4]	AMS BiCMOS	2.8 V	2.9 KS/s	8.18 + 9.71
	0.8- μm BYQ	2 V	0.7 KS/s	1 + 1.3

Oversampled converters such as sigma-delta converters are potentially viable for this application. Sigma-delta ADCs can be made to be low-power [5] for a given resolution and sampling rate, however they are complex– requiring sophisticated clocking and filtering. In addition, the oversampled clock needs to be much faster than the desired sampling rate. Generating the oversampled clock on each sensor node would likely offset any energy savings achieved in the rest of the ADC.

Continuing the survey of common architectures, integrating (single and dual slope) converters [5] possess many of the desired architectural features. They require very little analog circuitry, making them very low-power. However they require accurate timing which may be difficult to achieve without a high precision clock. It is unlikely that such a clock would exist on the mote since generating this clock could consume quite a lot of power due to the precision requirements. Another disadvantage is that the conversion speed is very slow, in addition to the fact that the conversion period varies with input signal. The variable conversion period complicates the overall system design for the sensor node as a whole as different ADC samples will take different amounts of time.

The charge redistribution successive approximation architecture [2], [3], [1] is a viable architecture for this application space. The general architecture of a general successive approximation ADC usually consists of a rail-to rail analog comparator, a digital-to-analog converter and a successive approximation register (SAR). In general, the SAR is designed into the digital circuitry. The DAC required in the ADC is designed based on a R-2R ladder. Thus, both of them are suitable for the standard CMOS technology VLSI implementation. However, realizing high-accuracy and rail-to-rail MOS comparator concurrently remains a problem because of MOS device mismatches [5], [6] and threshold voltage limitations [7]. Also the accuracy of a successive approximation converter depends on the matching accuracy of the on-chip passive components because the converter employs the ratio matched components as a precision reference element. In order to maintain ratio accuracy, such precision components require a large area and cannot be easily scaled down.

Algorithmic converters [6] offers all the advantages of the successive approximation architecture, while combining full flexibility to choose current as the information carrying quantity. Current-mode circuits offer the advantages of inherent low-voltage swing and no need for linear capacitors, as opposed to that used in switched capacitor techniques for voltage-mode algorithmic ADC's. Another advantage of algorithmic converter block is that it can be easily repeated to make a pipelined algorithmic converter by simply placing a current-mode sample and hold blocks (SH) in between each block [8]. The energy consumption depends on the number of blocks cascaded i.e. N, where N is the number of bits of resolution desired in the resulting conversion. Recently, current-mode circuit techniques which process the active signals in the current domain have been proposed to design the current-mode ADC [9], [7], [1].Thus, they are suitable for low-voltage applications. Though Nairn and Salama has demonstrated

a 6-bit current-mode algorithmic ADC [9] with very small chip area and low-power dissipation, enhancements were needed to further reduce the power consumption and to reduce the supply voltage without significantly increasing the chip area. Thus, the current-mode algorithmic ADC was chosen and the architecture was modified as to work with low-voltage and current supply as to have low-power consumption. The design presented makes use of the transistors operating in sub threshold region, so that the can work under low-voltage and low current supply.

IV. SUBTHRESHOLD REGION

One of the novel features of the design of the current-mode ADC proposed in this project is that it consumes ultra-low-power. Such low-power consumption can be achieved by many techniques which makes low-voltage application possible. Few of these techniques are using bulk-driven MOSFETs [8], floating gate MOSFETs [9] etc. But low-voltage alone is not sufficient to achieve ultra-low power, current consumption should also be lowered accordingly and moreover the above mentioned techniques have other issues associated with them, like higher input referred noise due to smaller equivalent trans conductance. To achieve ultra-low-power operation in this design, the transistors were operated in sub threshold or weak inversion region of operation so operation of MOSFET in this region, its modeling, its noise analysis and its leakage problem need to be discussed.

1.Operation in Sub threshold Region

Sub threshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate voltage is below Vth (threshold voltage). The weak inversion region is seen in Fig.4.1 as the linear region of the curve (semilog plot). In the weak inversion, the minority carrier concentration is small, but not zero.

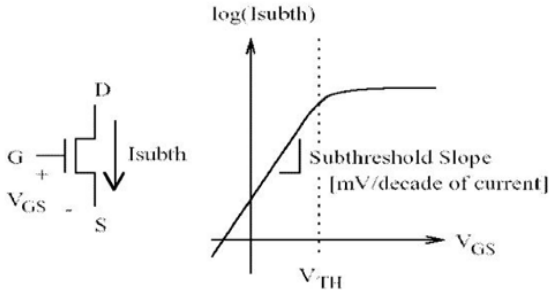


Fig. 5 Sub threshold current in a NMOS transistor.

The weak inversion region is shown as the linear region of the curve.

2 Variation of minority carrier concentration in the channel of MOSFET biased in weak inversion.

The component of the electric field vector E(Ey), being equal to, $\partial\varphi / \partial y$ is also small. With both the number of mobile carriers and the longitudinal electric field small, the drift component of the sub threshold drain-to-source current is negligible. Therefore, unlike the strong inversion region in which the drift current dominates, the sub threshold conduction is dominated by the diffusion current. The carriers move by diffusion along the surface similar to charge transport across the base of bipolar transistors. The exponential relation between driving voltage on the gate and the drain current is a straight line in a semilog plot of ID versus Vg (see Fig. 5.1). Weak inversion typically dominates modern device off-state leakage due to the low Vth. The weak inversion current can be expressed based on the following [4]:

$$I_{DS}=KP\frac{W}{L}(1+\text{LAMBDA}.V_{DS})\,(V_{GS}-V_{TH})^2$$

where Vth is the threshold voltage, and υ_T =kT/q is the thermal voltage. Cox is the gate oxide capacitance; 0 is the zero bias mobility; and m is the sub threshold swing coefficient (also called body effect coefficient). Wdm is the maximum depletion layer width, and tox is the gate

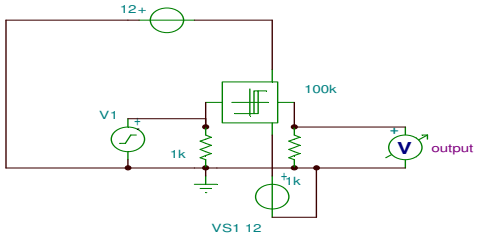
oxide thickness. Cdm is the capacitance of the depletion layer.

4.3 Modeling in Sub threshold Region

The accurate modeling of MOS transistors in moderate and weak inversion regions are not guaranteed as moderate region is considered just a transition region through which one fits an approximate curve. So couple of tests should be performed to verify the modeling of the MOSFET, which were finding in accordance with the required graphs. The graphs were obtained by simulating a NMOS transistor in Cadence, whose drain was given a fixed dc bias, source was grounded and gate voltage was swept over the entire range. The simulation was performed so as to confirm if the MOS device is modeled correctly for weak inversion region of operation. Fig 5.3 and Fig 4.4 confirmed the modeling. This was important since all the blocks in ADC are using transistors working in sub threshold region; hence the simulation performed on these blocks and as a result on the overall ADC will give the accurate results.

V. SIMULATION RESULTS

1. Design Of Basic Comparator



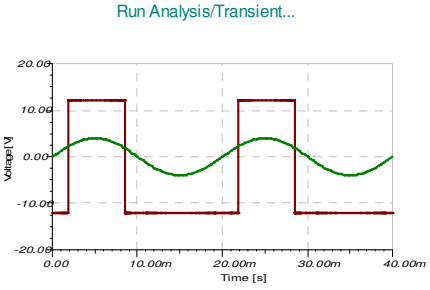


Fig. 6 Voltage and time curve

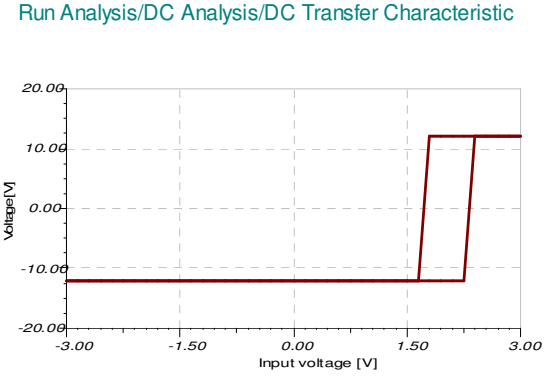


Fig. 7 Run time analysis

2. Proposed Circuit In ADC

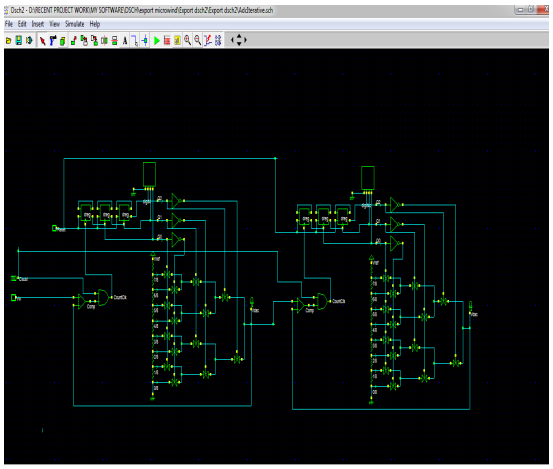


Fig. 8 Pipielining in 8BIT Repeated Counter InADC Display To Show 8bit Segment.

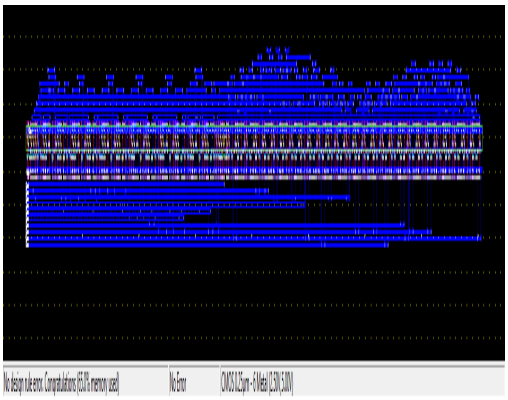


Fig. 9 Bit Pipeline in ADC Layout.

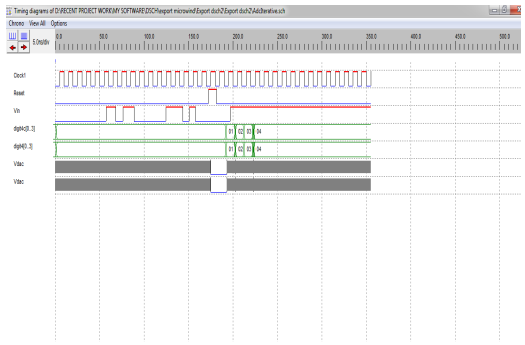


Figure 10 counter output in 8bit sar ADC.

3 Enhancement Report

The first graph presents the change in switching time with respect to variation in aspect ratio. It is important to see these results because it's the main thing which will affect the speed of the dynamic amplifier.

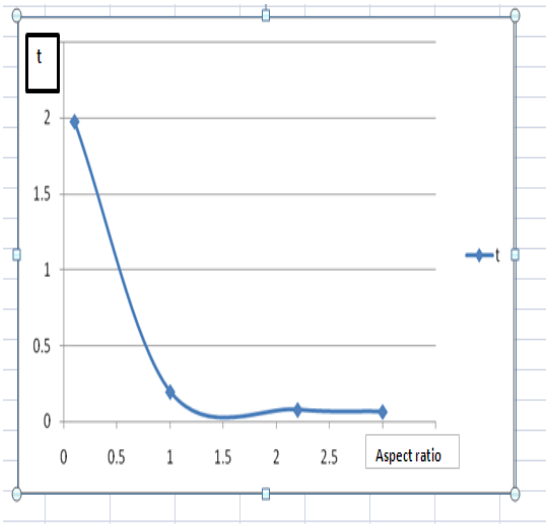


Fig. 11 Graph between switching time & aspect ratio.

From this graph it is very clear that as we increase value of aspect ratio the switching time decreases. Switching time is the time required to on or off the transistor. So that speed will increase because speed is indirectly proportional to time. For better results w=3l can be a good option.

Fig. 11 this graph represents the relation between drain current and aspect ratio for three different materials Ge, Si and GaAs. Their motilities are different; other things are constant for them.

Table 2 Result Compare to Various Research.

Architecture	Technology	Supply voltage	Sampling Rate	Power (mW)	Area (mm^2)
This Work	0.25-μm CMOS	1V	100 KS/S	0.204	0.187
Interpolated Pipeline Architecture	90 Nm CMOS	0.55 V	160 MS/S	2.43	0.25
Successive Approximation Technique	65nm & 90nm CMOS	1v & .5v	50ms/S	3.5 3.6	0.16
Differential Opamp Technique	0.18-μm CMOS	1.8v	20ms/S	0.7	0.19
Folded Cascode Technique	0.18-μm CMOS	1.8v	230 Ms/S	270	1.97
Switched-Opamp Technique	0.5-μm CMOS	1.5	5ms/S	1.6	1.3

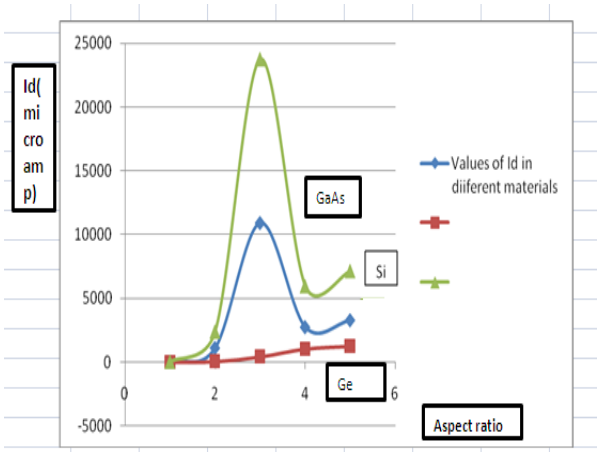


Fig. 12 Graph represents Comparison of three elements based on mobility

From this graph we can observe that GaAs is the best because its curve reaches at max.Some results which are drawn from analysis are as follows;

- The threshold voltage for the dynamic amplifier is decreased.
- Power consumption naturally will reduce.
- The input impedance decreases to some content.
- Before the triggering was at5 V, now it is reduced to 3 V.

- RAM, ROM can be designed easily.

Applications

- ADC where we deal with very low voltage swings
- Microstrip antenna can be designed.
- High speed processor or controller can be designed.

VI. Conclusion

This enables the use of dynamic amplifiers in a pipeline ADC. In addition, the dynamic amplifier offers both clock scalability and high-speed operation even with a scaled supply voltage. Using the above techniques, a 8 bit prototype ADC achieves a conversion rate of 160 MS/s with a supply voltage of 0.55 V. Therefore, the combination of interpolated pipeline architecture and dynamic residue amplifiers demonstrates the feasibility of ultra-low voltage high-speed analog circuit design. To implement the whole system a low-power and small size capacitance value sensing readout circuit is required. Also, it has to be integrated together with the back-end low-power current-mode ADC on the same chip. The low-power current-mode ADC has been designed and fabricated with TSMC 0.18um CMOS technology. In the simulation result, the power consumption for 8-bit ADC was 6 W, with a power supply of 0.65 V. The targeted specifications are met with the simulations in the schematic level and it has been shown that power consumption of the ADC using correlated level shifting is low.

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