International Journal of Scientific Research & Engineering Trends
Volume 4, Issue 1, Jan-Feb-2018, ISSN (Online): 2395-566X

Review Article of Basic ADC Design and Issue of Old Algorithm

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Abstract – **Analog to-digital converters (ADCs) are key design blocks and are at present embraced in numerous application fields to enhance computerized frameworks, which accomplish better exhibitions with regard the analog arrangements. With the quick progression of CMOS manufacture innovation, more signal processing capacities are actualized in the computerized space for a lower cost, bring down power utilization, higher yield, and higher re-configurability. Across the board use gives awesome significance to the design exercises, with these days to a great extent adds to the generation cost in coordinated circuit gadgets. This has as of late generated an extraordinary interest for low-control, low-voltage ADCs that can be acknowledged in a standard deep submicron CMOS innovation. Different cases of ADC applications can be found in information securing frameworks, estimation frameworks and digital correspondence frameworks likewise imaging, instrumentation frameworks. Subsequently, this work need to considered every one of the parameters and enhancing the related execution may fundamentally decrease the modern cost of an ADC producing process and enhanced the determination and configuration extraordinarily control utilization . This paper displays a 4 bit Pipeline ADC with low power dissipation executed in <0.18µm CMOS innovation with a power supply of 1.2V.**

Keywords – **Analog-to-digital converter (ADC), CMOS circuits.**

I. INTRODUCTION

As IC creation innovation has propelled, more analog signal processing capacities have been supplanted by computerized pieces ,analog to-digital converters (ADCs) hold an essential part in most current electronic frameworks on the grounds that most signals of intrigue are analog in nature and must to be changed over to computerized signals for additionally signal handling in the digital space.

There is wide range of ADC designs accessible relying upon the prerequisites of the application. Pipeline ADCs are a standout amongst other illustrations. Pipeline analog– to-computerized converters (Pipeline ADC) have as of late turned out to be extremely alluring in vitality effective direct determination/direct speed applications because of their insignificant dynamic analog circuit prerequisites. It normally create one piece for each clock cycle, the advantages are the low territory required for the usage. ADCs of this compose have great resolutions and very wide ranges. By consolidating the benefits of the progressive guess and blaze ADCs this compose is quick, has a high determination, and just requires a little bite the dust measure.

The pipeline analog to-computerized converter (ADC) is a promising topology for fast information transformation with reduced zone and productive power dissipation. Its speed of activity far outperforms that of serial-based structures, for example, progressive estimate or cyclic converters, while its bite the dust territory and power dissipation positively contrast with that of blaze and other more parallelized models. Pipelined ADCs are generally utilized as a part of the regions of remote interchanges, computerized endorser line analog front closures, CCD imaging digitizers, studio cameras, ultrasound screens, and numerous other fast applications.

Pipeline analog to-computerized converters (ADCS) speak to most of the ADC showcase for medium- to high-determination ADCS. Pipeline ADCS furnish up to 5Msps examining rates with resolutions from 8 to 18 bits. The Pipeline ADC engineering takes into consideration elite, low power ADCS to be bundled in little shape factors for the present applications. With ADC this work have composed 4 bit low power rapid Pipeline ADC with 0.18µm innovation.

II. REVIEW OF WORK

The primary recorded case of an ADC was a 5-bit, electro-optical and mechanical glimmer compose converter protected by Paul Rainey in 1921, used to transmit copy over broadcast lines with 5-bit heartbeat coded balance (PCM). The main all-electrical execution came in 1937 by Alec Harvey Reeves, this additionally had a 5-bit determination and the ADC was actualized by changing over the information signal to a prepare of heartbeats which was tallied to produce the paired yield at an example rate of 6 kS/s. Following this the progressive estimate ADC was created in 1948 by Black, Edson

Goodall to digitize voice to 5-bits at 8 kS/s. Likewise in 1948, a 96 kS/s, 7-bit ADC was created and it was generated and it was actualized utilizing an electron shaft with a sensor put on the opposite side of a cover. The veil had openings designed by the double weights with the goal that all bits were all the while identified, the example likewise utilized Gray coding of the yield keeping in mind the end goal to lessen the impact of mistakes in the most noteworthy piece (MSB) change, much as is done in present day rapid glimmer ADCS[12].

Following the improvement of the transistor in 1947 and the coordinated circuit in 1958, the ADC advancement proceeded in the 1960's with for instance a 8-bit, 10 MS/s converter that was utilized as a part of rocket resistance programs in the United States. Amid that decade, all the presently utilized rapid structures were generated incorporating Pipeline ADCS with mistake rectification. Business streak converters showed up in instruments and modules of the 1970S and immediately relocated to incorporated circuits amid the 1980S. The solid 8-bit streak ADC turned into an industry standard in digital video utilizations of the 1980S. Today, the blaze converter is principally utilized as a building obstruct inside sub running "pipeline"[9]. Utilizing Partial intensifier sharing topology, a 6-bit pipeline ADC, created in 0.35µm CMOS process. A 6-bit, 2.5 V streak ADC configuration has been accounted for new blaze topology and this new topology has just 2(N-2) + 2 comparators required. Here territory of the chip is vast and its required to limit it [10]. The AD7880 is a fast, low power, 12-bit A/D converter which works from a solitary +5V supply.

To begin with business converter, 1954 "DATRAC" 11-Bit, 50-kSPS SAR ADC Designed by Bernard M. Gordon at EPSCO. In the current years there has been a pattern in ADC research to utilize low precision analog parts which are made up for using digital blunder rectification. Due to their ubiquity, progressive estimate ADCs are accessible in a wide assortment of resolutions, testing rates, info and yield alternatives, bundle styles, and expenses. Numerous SAR ADCs now offer on-chip input multiplexers, settling on them the perfect decision for multichannel information securing framework. A case of current charge redistribution progressive estimate ADCs is Analog Devices' PulSAR® arrangement. TheAD7641 is a 18-bit, 2-MSPS, completely differential, ADC that works from a solitary 2.5 V control supply. The part contains a fast 18-bit inspecting ADC, an inward transformation clock, blunder amendment circuits, inner reference, and both serial and parallel framework interface ports. The AD7641 is equipment production line aligned and extensively tried to guarantee such air conditioning parameters as signal to-clamor proportion (SNR) and aggregate symphonious bending (THD), notwithstanding the more customary dc parameters of pick up, counterbalance, and linearity.

The inspiration driving this is analog outline have not possessed the capacity to profit by process scaling similarly as computerized rationale and in this way the generally area-cheap digital rationale is utilized to adjust for the deficiencies of costly analog circuits. For gadget unwavering quality reasons, the supply voltage should be diminished to guarantee door oxide trustworthiness after some time and keep p-n intersection from breakdown. Show day CMOS forms are making the progress from 3.3 V to 1.8 V supplies. The converter ought to work with high testing rate from a working supply as low as could reasonably be expected, to encourage combination with low-voltage, control productive computerized circuits.

III. Pipeline ADC Design

The pipeline ADC architecture combines the benefits of high throughput and an input capacitance bound by noise constraints. Typical pipeline architecture is illustrated in Figure 1. Each stage has the four elements of Comparator, a summer, multiplier, mux and transmission gate.

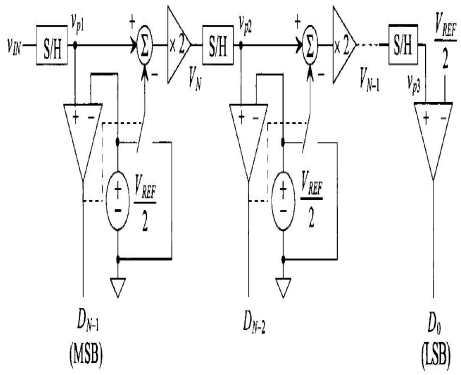

Fig 1 pipeline A/D converter

The pipeline ADC is an N-step converter, with 1 bit being converted per stage. Able to achieve high resolution (10-13 bits) at relatively fast speeds, the pipeline ADC consists of N stages connected in series (Fig.). Each stage contains a 1-bit ADC (a comparator), a sample-and-hold, a summer, and a gain of two amplifiers. Each stage of the converter performs the following operation:

a. After the input signal has been sampled, compare it to vref/2. The output of each comparator is the bit conversion for that stage.

b. If vm > vref/2 (comparator output is 1), vref/2 is subtracted from the held signal and pass the result to the amplifier. If vIN < vref/2 (comparator output is 0), then pass the original

input signal to the amplifier. The output of each stage in the converter is referred to as the residue.

c. Multiply the result of the summation by 2 and pass the result to the sample and- hold of the next stage.

A fundamental preferred standpoint of the pipeline converter is its high throughput. After an underlying dormancy of N clock cycles, one transformation will be finished per clock cycle. While the buildup of the principal organize is being worked on by the second stage, the primary stage is allowed to work on the following examples. Each stage works on the deposit go down from the past stage, in this manner taking into consideration quick transformations. The burden is having the underlying N clock cycle delay before the main computerized yield shows up. The seriousness of this drawback depends, obviously, on the application. One intriguing part of this converter is its reliance on the most huge stages for precision. A slight blunder in the primary stage spreads through the converter and results in a considerably bigger mistake toward the finish of the transformation. Each succeeding stage requires less exactness than the one preceding, so unique care must be taken while thinking about the initial a few phases.

The Pipelined ADC can be thought of as an amplitude- interleaved topology where errors from one stage are correlated with errors from previous stage. The basic block diagram implementation of an N-bit Pipelined ADC using the cyclic stages is as shown in Figure 2.

Instead of cycling the analog output of the 1 bit/stage section back to its input, we feed the output into next stage. The stages are clocked with opposite phases of the master clock signal. The comparator outputs are labeled digital in figure.

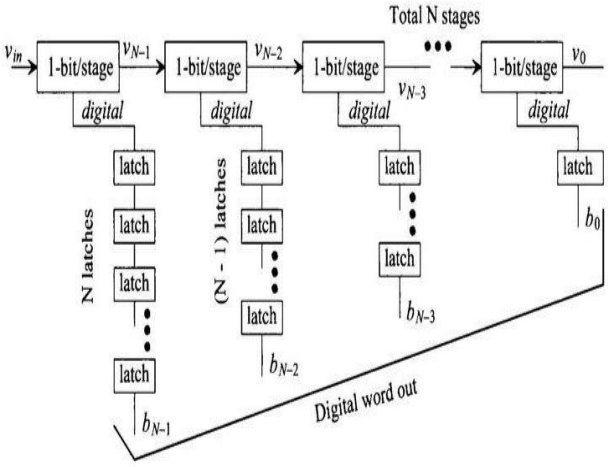

Fig 2. Pipeline ADC based on cyclic stages.

The digital comparator outputs are delayed through latches so that the final digital output word corresponds to the input signal sampled N clock cycles earlier. The first stage in figure must be N-bit accurate. It must amplify its analog output voltage, VN-1 to within 1 LSB of the ideal value. The second stage output, VN-2 must be an analog voltage within 2 LSB of its ideal value. The third stage output, VN-3 must be an analog voltage within 4 LSB of its ideal value.

Power dissipation in ADC

Power dissipation in CMOS logic arises from following

a. Switching current from charging and discharging parasitic capacitance.
b. Short circuit current when both N & P channel transistors are momentarily on at the same time.
c. Leakage current & sub threshold current.

Average dynamic power dissipated is given by :-

$$Pavg = Ctot * VDD^2 * Fclk$$

Notice that power dissipation is a function of clock frequency. A great deal of effort is put into reducing the Power dissipation in CMOS circuits.

Together with the scaling of process geometry, the supply voltage (squared term) is reduced in order to both reduce the digital Power dissipation and the rate of device degradation. Also we have to reduce short circuit current, sub threshold current, leakage current.

The basic problems coupled to SC, such as clock feed through from digital part through the switches, capacitor mismatch and op-amp non-idealities, have been taken into account during the design of the ADC. AS we are using 0.18µm technology, supply voltage is 1.2 V. Also due to clock redundancy Power dissipation is reduced.

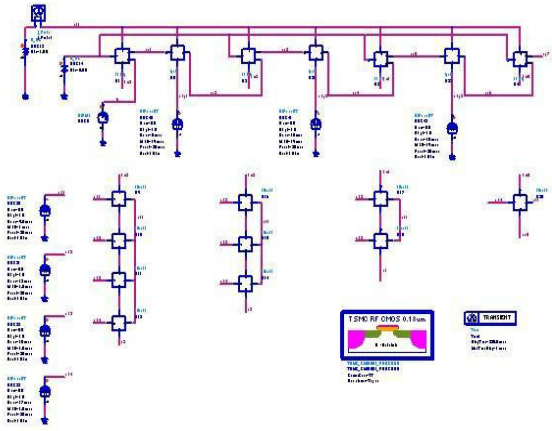

Fig 3 Pipeline Architecture.

IV. Circuit Implementation

With ADS and various designed components we have designed complete Pipeline Architecture shown in fig 3. And we got the simulation results shown in fig 4. And table 1 shows digital values for given analog voltage. For our Design of 4 bit resolution ADC digital code we are getting is as follows

Table 1 Digital Codes.

Input analog voltage	Q3	Q2	Q1	Q0
0000	0	0	0	0
0.0625	0	0	0	1
0.125	0	0	1	0
0.1875	0	0	1	1
0.25	0	1	0	0
0.3125	0	1	0	1
0.375	0	1	1	0
0.4375	0	1	1	1
0.5	1	0	0	0
0.5625	1	0	0	1
0.625	1	0	1	0
0.6875	1	0	1	1
0.75	1	1	0	0
0.8175	1	1	0	1
0.875	1	1	1	0
0.9375	1	1	1	1

1. Simulation Results

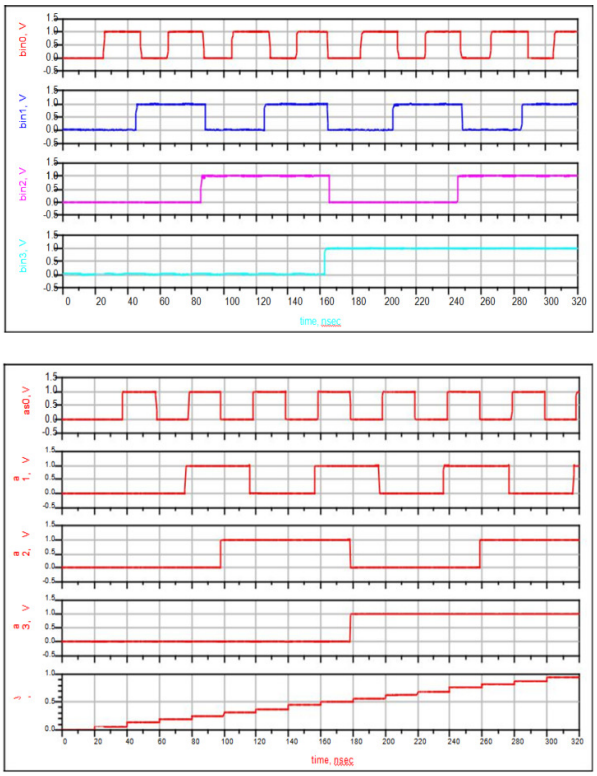

Fig 4 Simulation Results for Pipeline ADC

The ADC is fabricated in 0.18µm standard CMOS process with 4 bit rsolution. The value of the unit capacitor is 100fF. The static performance of the ADC is shown in Fig. 3. ADC operats at 1.2v. The DNL and INL of the ADC are a measurement factor of linearity.

2. Pipeline ADC vs other ADCs

Power dissipation of Pipeline ADCs varies with the sampling rate unlike Flash and SAR architectures. Hence find applications in PDAs.

The SAR ADC's are low power consumption, high resolution, and accuracy. In a SAR ADC, increased resolution comes with the increased cost of more-accurate internal components.

Flash ADC is much faster, less accurate and takes more silicon area due to the number of comparators 2N for N bit resolution.

Oversampled/Σ-J ADCs have low conversion rates, high precision, averaging noise and no requirement for trimming or calibration even up to 16 bits of resolution.

V. Conclusion

ADC is the key design Block in present day microelectronics digital correspondence framework. With the quick progression of CMOS creation innovation and proceeded with expansion of blended analog and digital VLSI frameworks, the requirement for little estimated, low-power and fast analog to-computerized converters has expanded.

With an expanding pattern to a framework on-chip, an ADC must be actualized in a low-voltage submicron CMOS innovation to accomplish low assembling cost while having the capacity to incorporate with other digital circuits. So this work have proposed low power ADC. From various ADC designs accessible Flash ADC is having the disadvantage of substantial chip zone n high power dissemination and Pipeline ADC has complex circuit. The Pipeline ADC is best reasonable for low power application.

For outlining reason this work have utilized Digital Designing System. The Pipeline ADC center is made by comparator, Transmission Gate, and pipeline control rationale; these parts have been composed focusing to satisfy a few imperatives on necessities, for example, low power dissipation, the balances because of jumble. From the results presented we could conclude that conversion is performed without missing codes and a low-power high speed 4-bit Pipeline ADC in a 0.18µm CMOS process with a 1.2 V supply voltage is designed.

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