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Low Read Power Delay Product Based Differential Eight Transistor SRAM cell

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***Abstract* – SRAM is designed to provide an temporary storage for Central Processing Unit and replace Dynamic RAMs in systems that require very low power consumption. Low power SRAM design is critical aspect since it takes a large fraction of total power and die area in high performance processors. This paper include the work on eight transistor SRAM cell that offer smaller read power delay product due to cascading of pull-down transitor during read. Proposed eight transtor SRAM cell offers 28% (74%) smaller read '0' ('1') than exiting 7T. The SRAM cell read and cycle is characterized at 45nm technology using SPICE EDA tool.**

***Keywords* – Cache Memory, Hold Power, Read/Write Access Time, read cycle and write cycle.**

I. INTRODUCTION

Scaling in Silicon technology, usage of SRAM Cells has been increased to large extent while designing the embedded Cache and system on-chips in CMOS technology. Power consumption, packing density and the speed are the major factors of concern for designing a chip. The need of portable battery operated high speed devices like notebook, laptop, personal digital assistants, cellular phones, etc are involved in daily routine. High speed portable devices require primary storage that responds faster. For that purpose, static random access memory is used, which is faster and refreshing is not needed again and again. Dynamic power dissipation and leakage current are the main issues of high speed SRAM cells because this unwanted power dissipation reduces the battery backup life of portable devices. So it is required to have a SRAM cell design, having both low static and dynamic power dissipations. Supply voltage is scaled to maintain the power consumption within limit. However, scaling of supply voltage is limited by the high performance requirement. Hence, the scaling of supply voltage only may not be sufficient to maintain the power density within limit, which is required for power sensitive applications. Circuit techniques and system level techniques are also required along with supply voltage scaling to achieve low power designs [1].

Aggressive scaling of the devices not only increases the sub threshold leakage but also has other negative impacts such as increased drain induced barrier lowering (DIBL), threshold voltage roll off, reduced on current to off current ratio, and increased source to drain resistance [2]. V_{th} roll off increases the dependence of V_{th} on the channel length. A small variation in channel length might result in large threshold voltage variation, which makes device characteristics unpredictable. To avoid these short channel effects, oxide thickness scaling and higher and non uniform doping need to be incorporated [3] as the devices are scaled. The low oxide thickness gives rise to a high electric field, resulting in considerable direct tunnelling current [4]. Higher doping results in a high electric field across the reverse biased p–n junctions (source-substrate or drain substrate) which cause significant band to band tunnelling of electrons from the valence band of the p region to the conduction band of the n region. Peak halo doping (P+) is restricted such that the BTBT component is maintained reasonably small compared to the other leakage components. In another technique [5], a low area overhead adaptive body bias circuit is proposed to compensate for aging and process variations to improve the SRAM reliability and yield. The p ABB circuit consists of a threshold voltage sensing circuit and an on chip analog controller for power reduction. A multi threshold complementary metal oxide semiconductor technology provides low leakage and high performance operation by utilizing high speed, low threshold voltage transistors during active mode and low leakage, high threshold voltage transistors during sleep mode, which reduces the static power dissipation of the SRAM circuit [6, 7].

In this work, 6T[8] and 7T[9] topologies are studied and compared with proposed work. 6T SRAM cell suffer with severe power dissipation, higher read/write delay and poor power delay product . The rest of the paper is organized in the following order. Section II presents literature review on existing low power SRAM cells, The proposed work discussed in section III, Result analysis are discussed and in Section IV. Finally, the concluding remarks in Section V.

II. LITERATURE ON SRAM

This article presents the review of 6T and 7T SRAM cell.

2.1 6T SRAM cell: Fig. 1 shows the circuit diagram of a conventional SRAM cell [8, 10]. Before the read operation begins, the bit line (BL) and bitbar line (BLB) are precharged to as high as supply voltage Vdd. When the word line (WL) is selected, the access transistors are turned on. This will cause a current to flow from supply voltage (Vdd) through the pull up transistor TP1 of the node storing ''1''. On the other side, current will flow from the precharged bitbar line to ground, thus discharging bitbar line. Thus, a differential voltage develops between the BL and BL. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output.

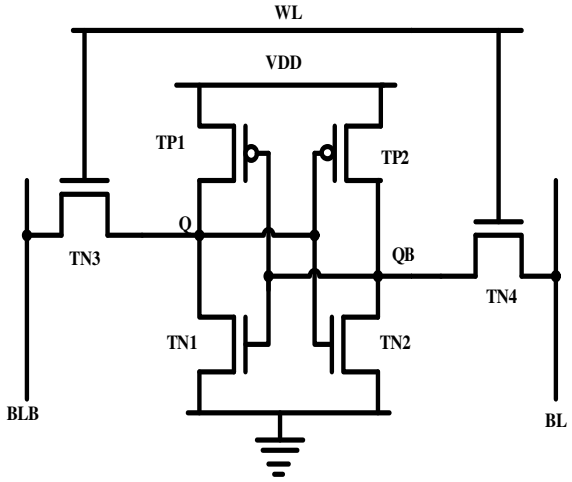


Fig.1 Conventional 6T SRAM cell[10]

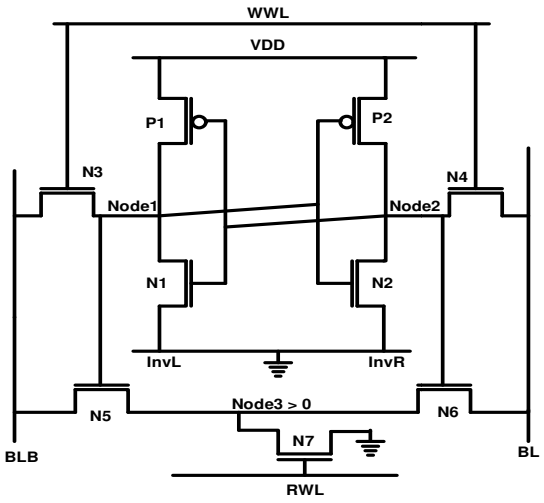


Fig.2 9T SRAM Cell[11].

2.2 9T SRAM cell: The 9T SRAM [11] is shown in Fig.2. Write occurs just as in the 6T SRAM cell. Reading occurs separately through N5, N6 and N7 controlled by the read signal (RWL) going high.This design has the problem of the high bit line capacitance with more pass transistors on the bit line.

2.3 Fully Differential Low Power 10T SRAM: The fully differential low power 10T SRAM [12] bit cell is shown in Fig.3. The design strategy of cell is the series connection of a tail transistor. The gate electrode of this device is controlled by the output of an XOR gate, inputs of which are tapped from write word line (WWL) and read word line (RWL) control signals coming from the WWL and the RWL drivers. The XOR gate and the tail transistor are shared by all the cells in a row. The tail transistor has to be appropriately up sized for sinking currents from all the cells in the row. Without this read buffer, a cell with such small drivers and series connected tail transistor would exhibit unacceptably low read static noise margin (RSNM), resulting in read instability.

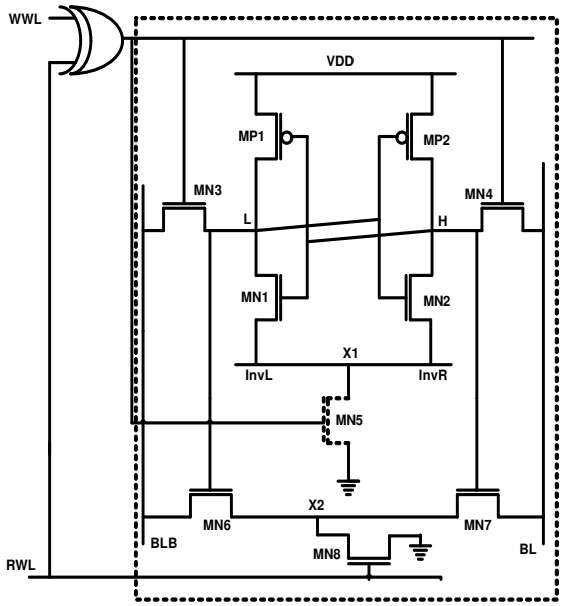


Fig.3. Fully Differential Low Power 10T SRAM (LP10T)[12]

2.4 Schmitt trigger based 10T SRAM cell (ST10T): The Schmitt trigger based 10T SRAM cell [13] is shown in Fig.4. Extra devices MN5/6/7/8 of ST10T are of minimum width. This extra transistor makes read faster than LP10T.

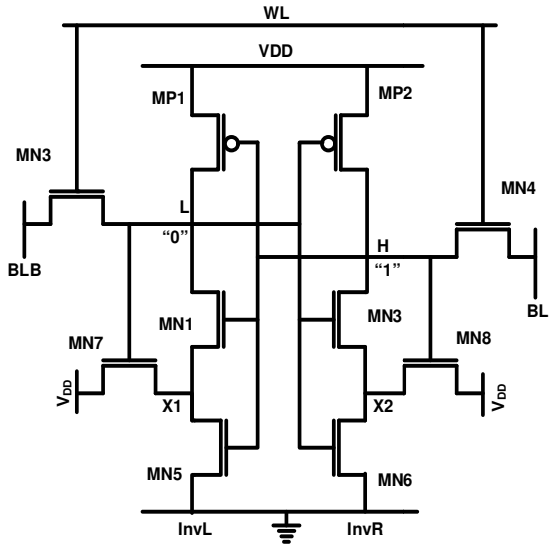


Fig.4 Schmitt trigger based 10T SRAM cell (ST10T)[13]

2.5 Write-and-Read-enhanced 8T SRAM cell (WRE8T): Fig. 5 shows circuit diagram of our proposed SRAM cell[14]. In this cell, M5 is write access transistor and M6 is for read access. Having individual access transistors in our cell, it is possible to increase size of write access transistor to improve write-ability and choose minimum size for read access transistor to enhance read stability, whereas in 6T there is a conflict while sizing the access transistors. In the proposed SRAM cell, the added pMOS and nMOS transistors (M7, M8) become OFF during write operation. This interrupts VDD and GND connections of the left inverter in the cell. Thus, left inverter becomes weaker during write operation, and a relatively stronger write access transistor can easily write the input to our cell.

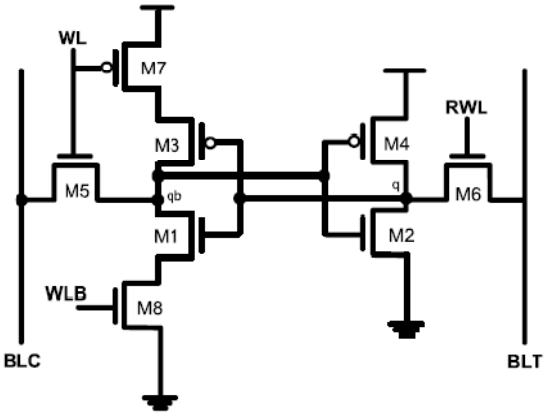


Fig.5 Write-And-Read-Enhanced 8T SRAM cell (WRE8T)[14].

In WRE8T, before read operation bit-line of read (BLT) is precharged to VDD, and then by asserting RWL signal, M6 (Fig. 5) becomes ON and according to the stored data at node q, the capacitance of BLT bit-line is discharged or remains unchanged.

2.6 Differential 7T SRAM based Memory Cell: Existing 7T SRAM[9] cell varies with the design. Here, the two cross coupled inverters with two pMOS (M1, M3) and two nMOS (M2, M4) were used. The gate transistors, M5 and M6 are connected to point Q and Qbar. Transistor M7 is connected parallel to transistor M4 and its gate is attached with RWL line which activates only on read operation. When WRL is high,
access transistors M5 and M6 are ON are read or write operation is performed. For holding data or standby mode WRL gets low and transistors M5, M6 and M7 stay OFF.

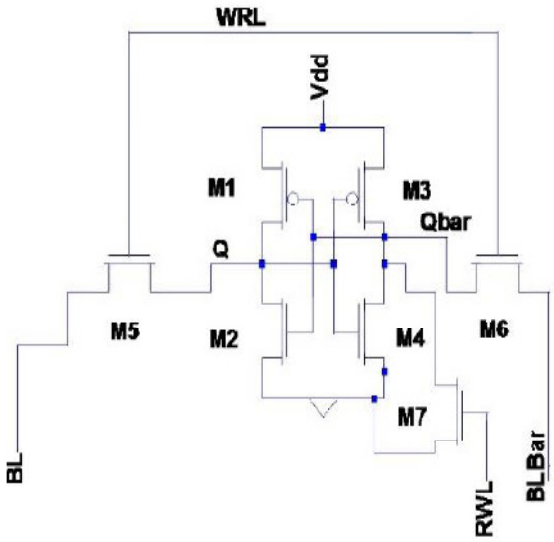


Fig.6 Fully differential 7T SRAM cell[9]

III. PROPOSED WORK

Proposed 8T SRAM cell varies with the design. Here, the two cross coupled inverters with two pMOS (M1, M3) and four nMOS (M2, M4, M7, M8) are used to form back to connected pair during read operation only. While M2 and M4 operates in sub-threshold region during write and standby mode. The gate transistors, M5 and M6 are connected to point Q and Qbar. Transistor M read is connected between pull down device (M2 and M4) and ground in stack configuration. access transistors M5 and M6 are ON during read or write operation. While M_{read} is common for pair of SRAM cell in a row, therefore overall penalty on layout area will be negligible.

Table-1 Status of SRAM control signal during read/write/Hold mode.

Operation	WL	RWL
Read	VDD	VDD
Write	VDD	GND
Idle or hold	GND	GND

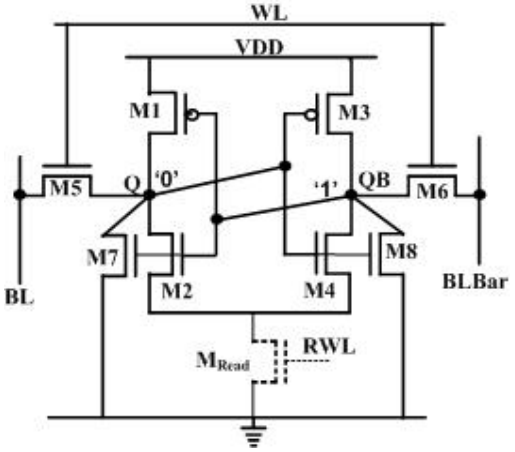


Fig.7 Proposed Differential 8T SRAM Cell

IV. RESULTS AND ANALYSIS

SRAN can be characterized on the basis of following parameters such as read delay, read power, read PDP, write delay, write power, write PDP and no. of transistor used for cell design.

4.1 Read and Write Power Dissipation: The power in embedded cache is an alarming issue in deep-submicrometer technology. In most frequently used SRAM cell read and write power should be smaller.

4.2 Read Delay:TRA (read access time or read delay) is estimated from the time when RWL (WL) (wordline) is activated to the time when bitline (BL)/bitline bar(BLB) is discharged by 50 mV from its initial high level [14]. The 50-mV differential between BL and BLB is good enough to be detected by a sense amplifier, thereby avoiding misread [14], [15]. It is observed that 6T and WRE8T have smallest read access time. The read delay must be smaller.

4.3 Write Delay:TWA (write access time or write delay) is estimated as the time required for writing "0" to storage node "L" from the time when WWL(WL) is activated to the time when "L" falls to 10% of its initial high level (i.e., its 90% swing). Similarly, TWA for writing "1" to "L" is estimated from the time when WWL (WL) is activated to the time when "L" rises to 90% of its full swing from its initial low level. This avoids miswrite. All the SRAM cell shows small and equal write access time except WRE8T. It must be small for higher operating speed.

4.4 Read and Write PDP: Delay and power dissipation can not independently define the merits of SRAM cell. Sometimes SRAM cell offer lower delay but higher power dissipation or just opposite of that. So, the read/write power and delay product (equivalent to energy) is the best way to characterize SRAM cell. Read/Write PDP of practical SRAM should be smaller.

4.5 Layout Area: It is observed that 6T has smallest layout area. Layout area provide information about bit line capacitance, internal node capacitance, read access time, write access time and packaging density of SRAM.

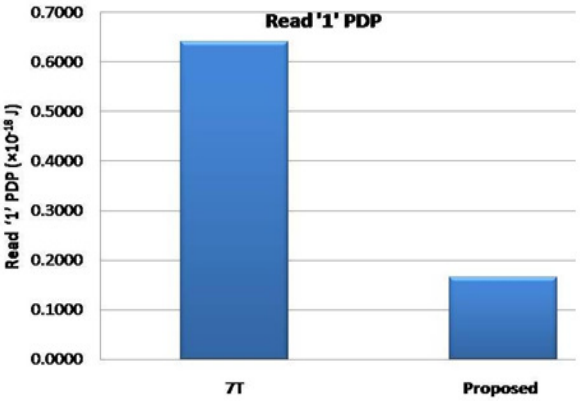
4.6 Result Analysis: SRAM cells are compared on the basis of following parameters such as read delay, read power, read PDP, write delay, Write Power, write PDP and Transistor Count as shown in Table-2 and Table-3. In Table-2 and Table-3, we will compare the results of conventional 6T, 7T and proposed at 45nm technology for read and write operation. Proposed eight transtor SRAM cell offers 28% (74%) smaller read '0' ('1') than exiting 7T. The SRAM cell read and cycle is characterized at 45nm technology using SPICE EDA tool. The graphical comparisons of existing 7T vs Proposed is shown in Fig. 8.

Table-2: Read and write '1' performance parameter comparison at 45nm technology

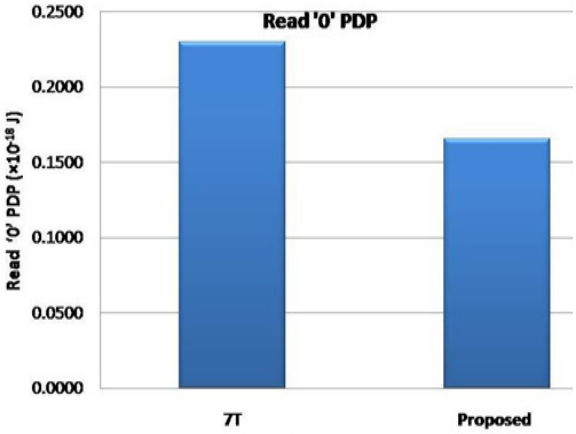
Circuits	Read Delay (ps)	Read Power (µW)	Read PDP (fJ)	Write Delay (ps)	Write Power (µW)	Write PDP (fJ)	Transistor Count
6T	0.04	-	-	0.11	-	-	6
7T	0.04	16	0.64	0.09	15	1.35	7
Proposed	0.756	0.219	0.165	8.23	0.25	2.02	8

Table-3: Read and write '0' performance parameter comparison at 45nm technology

Circuits	Read Delay	Read Power	Read PDP	Write Delay	Write Power	Write PDP	Transistor Count
6T	0.04	-	-	0.07	-	-	6
7T	0.01	23	0.23	0.09	20	1.8	7
Proposed	0.76	0.219	0.165	8.23	0.246	2.02	8



(a)



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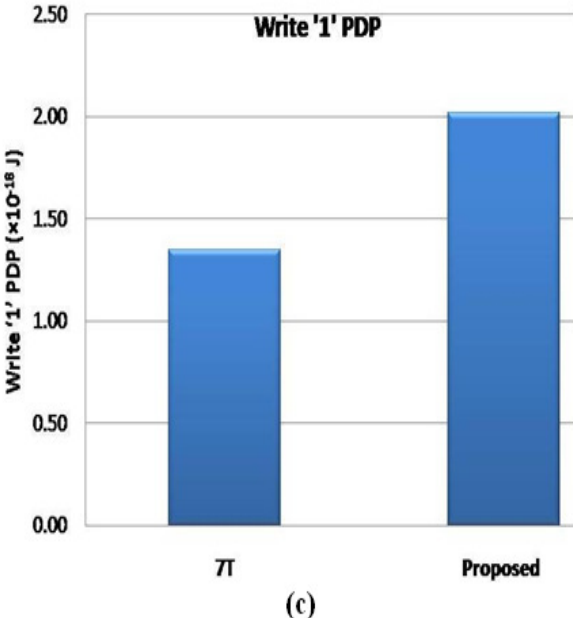
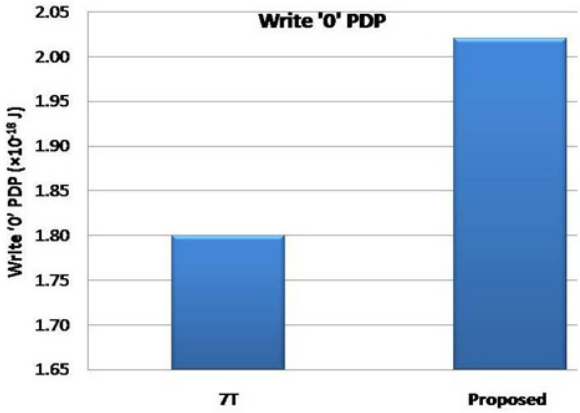


(c)



(d)

Fig. 8 PDP comparison of (a) Read '1', (b) Read '0', (c) Write '1' and (d) Write '0' operations.

V. CONCLUSION

Many SRAM cell is reviewed in literature section. But in 7T cell had an extra NMOS transistor connected in parallel with pull-down transistor compared to conventional 6T. With this transistor the leakage current during hold operation can be increased and discharging the storage node gets accelerated. The 7T cell performs better in both read and write mode. Proposed eight transistor SRAM cell offers 28% (74%) smaller read '0' ('1') than exiting 7T. The SRAM cell read and cycle is characterized at 45nm technology using SPICE EDA tool.

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