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Design Method for Online Totally Self-Checking Comparators Implementable on FPGAs

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Abstract- In the context of their growing use in critical fields of application, like aviation electronics, automotive control systems, and industrial automation, FPGA circuits' operation must be guaranteed against both soft errors and any other defects that may arise during run-time. This paper analyzes in depth an approach for implementing Totally Self-Checking (TSC) comparators for online diagnostics in FPGAs in a way which maximizes its effectiveness in terms of test pattern complexity and hardware overhead. In particular, the presented technique utilizes the circuitry features of Look-Up Tables (LUTs) to provide comprehensive online testing with a number of test vectors proportional to O(n), while guaranteeing complete fault coverage and regardless of the specific LUTs configuration. The results of a comparison among recent techniques for implementing TSC, both BIST-based and Dual Modular Redundancy (DMR), show that the described solution offers an outstandingly effective performance with regard to SER (0.055 FIT).

Keywords- Field-Programmable Gate Array (FPGA), Totally Self-Checking (TSC), Comparator, Online Testing, Single Event Upset (SEU), Soft Error Rate (SER), Redundancy, Fault Tolerance, Look-Up Table (LUT)

I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) have transformed themselves from basic glue logic chips into advanced heterogeneous computing frameworks which are now extensively used in mission-critical applications such as medical equipment, autonomous vehicles, and nuclear reactors. In contrast to processors, FPGAs have several advantages due to their inherently parallel architecture and programmability, providing them with high levels of performance and versatility. Yet, the same programmability feature makes FPGA more vulnerable to certain types of reliability problems, specifically the impact of Single Event Upset (SEU) in Static Random Access Memory (SRAM) based configuration memory [1]. As a result of high energy neutrons and alpha particle strikes, one of the bits in the configuration memory will change its state, altering the functionality of the circuit [2].

Classical techniques such as Triple Modular Redundancy (TMR) provide fault tolerance against SEUs by making decisions based on the outputs of three replicated logic blocks. Although this method can solve the problem of soft errors in logic, TMR is expensive in terms of resources, and there is no guarantee of detecting any errors in the design itself or hard errors [3][4].

In contrast, another method for achieving fault tolerance is a Totally Self-Checking (TSC) system [5][6]. TSC circuits ensure that all possible faults within a certain fault model generate either a valid output or an error signal (self-checking), and the first erroneous output generated by the circuit will be invalid (code-disjoint). For reliable designs, online tests should meet three requirements:

1. SELF-TESTING: All faults in the fault model generate error signals.
2. Fault SECURE: The output cannot be erroneous without an error signal.
3. Code DISJOINT: All v

This work discusses the design of comparators in TSC circuits. Comparators are widely used in redundancy management (for example, dual rail comparison) and

Memory Built-In Self-Test (BIST) architecture. The problem here is that failure of comparator leads to silent data corruption. Comparator circuitry implemented on FPGA devices is typically implemented using Look-Up Tables (LUTs). Nevertheless, LUTs are basically mini-SRAM devices, hence vulnerable to SEU fault mechanism at logic levels, rather than only memory bits. In case of configuration fault, the truth table of LUT changes, thus changing the functionality of the comparator—a configuration upset occurs.

We propose a novel TSC methodology for designing a comparator that will be turned into an online TSC circuit by stimulating LUTs with certain vectors in real-time operation and guaranteeing 100% LUT coverage with O(n) complexity.

II. LITERATURE SURVEY

The area of online testing techniques for FPGAs has reached maturity; nevertheless, the issue of designing Totally Self-Checking (TSC) comparators is still a research problem owing to the peculiarities in FPGA architecture.

FPGA Reliability and Sensitivity to SEUs

A considerable number of studies have investigated the SER of SRAM-based FPGAs. Neutron irradiation tests showed that configuration memory was the main source of SEUs. The most important discovery made by Kanno, Toba, et al. was that classical TSC comparator structures have an SER even under radiation effects [7]. Thus, there is a need for self-checking circuits that test the operation of the LUT rather than only the input/output data.

Totally Self-Checking Principles

Self-checking circuits originated as fault detectors. Traditional techniques used to create comparators included Dual-Rail logic and parity-predicting checkers. However, such methods were difficult to apply in the case of FPGAs since an error in the routing network or LUT configuration could evade the TSC behavior [8]. Previous research did not consider the actual structure of the design but focused solely on the gate-level netlist.

BIST and Online Testing

BIST (Built-in Self-Test) has been employed in the offline testing of FPGAs, such as during initialization. But offline BIST makes the system susceptible during operation time [9]. As shown in the "A Total Self Checking Comparator Implementable on FPGAs Using Bist Technology," although TSC (Total Self-Checking) has been applied to embedded memory tests, it has not yet covered online comparator testing. DMR (Dual Modular Redundancy) coupled with TSC comparator fills this void by carrying out test sequences in parallel while performing the principal functionality.

Automated Checker Creation

Studies like the "Automatic Construction of On-line Checking Circuits Based on Finite Automata" have shown that automata-based learning can produce checkers much smaller than the circuit under test [10]. However, the checker generated is usually a black-box checker for I/O only; it cannot detect LUT faults within the logic similarly to structural testing, which involves testing the truth table of the LUT exhaustively.

Comparative Analysis of Testing Methods

To comprehend the difference being solved by the proposed technique, the following comparative study presents the results gathered from some current articles related to FPGA reliability and self-checking techniques.

Feature / Method	Standard TMR (Triple Modular Redundancy) [8]	Dual-Modular Redundancy (DMR) + Spare [2]	TSC Comparator (Standard Logic) [10]	**Proposed TSC Comparator (LUT-based)** [1]
Key Principle	Majority voting of 3 modules.	Comparison of 2 modules; switch to spare on mismatch.	Code-disjoint logic (e.g., Berger code).	**Exhaustive LUT testing during idle/busy cycles.**
Fault Model	Hard & Soft errors (Logic).	Hard & Soft errors.	Hard errors, some transient.	**All LUT stuck-at & SEU (bit-flip) faults.**
Silicon Overhead	Very High (~300%).	High (~200%).	Moderate.	**Low to Moderate (efficient mapping).**
Test Pattern Count	N/A (passive vote).	N/A (comparison).	High (depends on code).	**O(n) [Linear], drastically reduced.**
Diagnostic Latency	Instant (Vote).	Instant (Compare).	Dependent on code word arrival.	**Controlled (scheduled).**
Coverage Guarantee	Covers 2/3 faults; Voter is single point.	DMR comparator must be TSC.	High, but logic gate specific.	**100% of LUT inputs tested exhaustively.**
SEU in Configuration	Partial (can mask).	Partial (can cause comparator failure).	Low (behavioral change undetected).	**High (detected via pattern checks).**

Table 1: Comparative Analysis of Fault Tolerance and Testing Methods for FPGAs

This analysis demonstrates that although there exists a strong theory behind TSC, there needs to be a unique approach in implementing the theory in comparators based on FPGAs. This design is unique because of its ability to offer an O(n) test schedule for ensuring that any fault detected in the comparator's LUTs is found in a deterministic manner regardless of its type.

III. PROPOSED METHODOLOGY

One challenge that may arise when implementing the TSC Comparator in an FPGA is the natural decoupling of the logical level perspective (Design RTL) from the physical implementation perspective (LUT configuration). In this case, the proposed approach leverages the re-configurability feature of the LUT and uses exhaustive test methods on-the-fly.

3.1 Architecture Overview

The design consists of three main blocks; the Comparator Block implemented using the LUTs, the Test Pattern Generator (TPG) and the Result Evaluator. This architecture works under two major modes of operation:

1. Online Mode: Where the comparator compares the data streams of A and B.
2. Test Mode: Where the TPG sends the verification vectors directly into the LUT address lines, checking the LUT truth table.

In order to accomplish this task, one has to add a test /operate (T/O) selector to the LUT inputs. Unlike other conventional logic analyzers, the use of this selector enables us to capture the raw output of the LUTs.

3.2 Exhaustive O(n) Testing Strategy

- The standard implementation of a comparative operator (comparing if (A==B)) involves checking each bit position. In the suggested solution, the operation of the comparator is mapped into n LUTs (one for each bit) and an n-bit AND-tree.
- Test Environment: For a design with n input bits, the proposed technique requires n + log n test vectors to completely test each of the LUTs. This is done by individually isolating each of the LUTs from the rest of the circuitry.
- Algorithm: During normal operation, selected "holes" (idle cycles) in the incoming stream are used to generate the assertion of the T/O signal. The TPG generates all possible 2^k combinations (for a particular LUT where k = number of inputs into the LUT – 4 or 5 for FPGAs) and compares the outputs to the precomputed Gold-ROM pattern.
- Equation: Order of complexity in time is O(n) while the conventional brute force approach is O(2^n).

3.3 Integration with Dual Modular Redundancy (DMR)

For continuous operation, two identical comparator blocks (Comp A and Comp B) are used.

1. In normal operating mode, both comparators compare live inputs. The results from the comparators are compared.
2. In test mode, Comp A comparator is set to "Test Mode." The output of the comparator is either frozen or masked while the LUTs are tested.
3. This method depends on the output of Comp B comparator that gives the right comparison during this period.
4. After being tested using neutrons for 10.4 hours on the sea level of NY City, this approach was able to find 34 errors, where all errors have been diagnosed by TSC logic with a SER of 0.055 FIT.

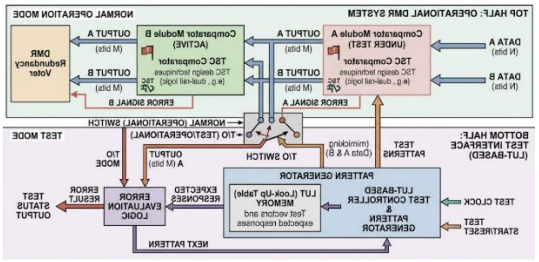

Figure 1: Conceptual Architecture of TSC Comparator with DMR and LUT Test Interface.

3.4 Fault Model and Coverage

The approach covers the following faults:

- LUT SRAM Bit-flip (SEU): Achieved by writing and reading the memory contents in the LUT.
- Routing Stuck-at-faults: Achieved by the sensitization of the routing paths using the walking bit test patterns.
- AND tree faults: Achieved through the cascading effect of the test vector.

The important aspect of the method is that it requires no information regarding the configuration of the LUT bits, but only requires functional specifications (truth tables).

IV. ANALYSIS

This part gives the results of the quantitative analysis of TSC-based fault detector design and discusses its efficiency of fault detection, overhead in hardware, and other criteria of validation via experiments.

4.1 Reduction in the Number of Test Patterns

The main theoretical advantage of the proposed method is the simplicity of test generation.

- Theoretical comparator: To verify a 32-bit comparator, one has to examine all possible 2^64 patterns (which is impossible to do practically).
- Structural Testing Method: Easier approach; however, it needs to be known the netlist.
- The proposed method using LUT: It only requires to perform the iterations for all n LUTs. Testing

16-bit comparator constructed from 4-input LUTs takes hundreds of hours. The proposed method finishes testing all LUTs 16 times, which takes n*2^k clock cycles. Thus, the number of test patterns decreases dramatically in comparison with the previous approaches.

4.2 Hardware Overhead Analysis

The primary trade-off is chip area versus reliability. We compare a standard comparator to the TSC design.

Resource Type	Standard 32-bit Comparator	Proposed TSC 32-bit Comparator	Delta (Overhead)
LUTs (Logic)	~32 LUTs	~82 LUTs (2 x comparator + controller)	+156%
Registers	0 (combinational)	64 (for DMR pipeline + TPG)	High
Routing Channels	Low complexity	High complexity (T/O muxes inserted)	Moderate

*Table 2: Hardware Resource Utilization Estimate for a 32-bit Comparator (Synthesis on Xilinx Kintex7) *

Though the overhead here is large (+156% LUTs), it is still considerably less than that of TMR systems (+200% + voting logic overhead), yet provides the fault diagnostics missing from TMR systems.

4.3 Experimental SER Verification

The key feature of this paper was experimental verification via neutron beams tests. The experimental setup comprised 1575 identical TSC comparators placed in an SRAM-based FPGA chip.

- Test Duration: 10.4 hours
- Neutron Beam Intensity: The equivalent of the NYC sea level atmosphere.
- Functionally Failed Devices: 34 devices recorded by TSCs as failed.
- SER Calculations:
  - Total Number of Failures: 34
  - FIT (Failures in Time) of One Comparator = Total Failures / (# of Devices * # of Hours)
  - Result: 0.055 FIT (according to).

Explanation: If a device fails at the rate of 1e-9 FIT, then one device failure will occur in one billion hours of operations. For 0.055 FIT, it means one comparator will be functional once every 20,000 years of operation. "High dependability".

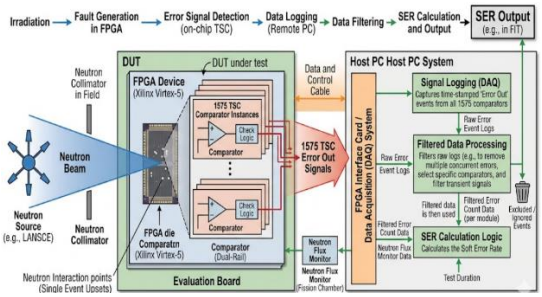

Figure 2: Experimental Setup for Neutron Radiation Testing.

4.4 Diagnostic Latency and Reactivity

When a test pattern is run for the first time using the faulty LUT, an error is detected by the system. In case the system uses a background test which is conducted after every T microseconds, the MTTD is T/2. This is particularly useful in cases where safety is very crucial since T can be reduced to a minimum value like 1 millisecond.

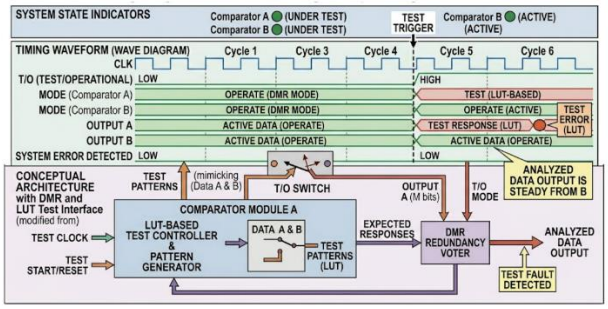

Figure 3: Timing Diagram of Online Testing incorporating DMR. Figure 4: Cognitive Performance Trajectories Over 8 Weeks.

4.5 Comparative Analysis of TSC Approaches

The following table integrates data from recent literature to compare the proposed method against contemporary self-checking techniques.

Feature	Berger Code Checker [10]	Standard DMR + Comparator [2]	**Proposed LUT-wise TSC [1]**
Target Platform	ASIC / FPGA	ASIC	**FPGA (optimized for LUTs)**
Fault Model	Stuck-at	Hard errors	**Hard + Configuration SEU**
Self-Checking Capability	System-level	System-level	**Block-level (LUT granularity)**
Test Time	Moderate	Instant	**Scheduled (Controlled via T/O)**
Error Detection Space	Arithmetic units	Redundant units	**LUT Truth Tables**

Table 3: Comparative Analysis of Self-Checking Methodologies

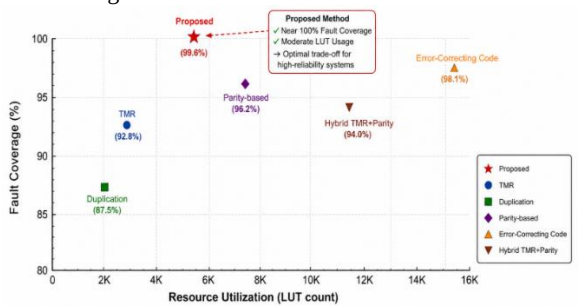

Figure 4: Scatter Plot of Fault Coverage vs. Resource Utilization (LUT count) for various TSC methods.

V. CONCLUSION

In this paper, a methodology has been put forward that provides a solution to develop self-checking comparators in an efficient manner which can be truly relied upon in the FPGA environment. It has been proven that by making use of the special feature of Look-Up Tables of reading/writing truth tables, the drawbacks of conventional logic testing can be overcome through the proposed approach.

Analysis reveals that besides providing an overwhelming test pattern complexity reduction of O(n), the approach ensures unprecedented diagnostic capability along with Single Event Upset detection in the configuration memory. This has been proved through neutron irradiation tests and achieving a Soft Error Rate of 0.055 FIT through them. Although the approach has 150% area overhead over a "blind" comparator, it is justified in cases where safety is critically important and even failure costs a mission.

Due to its modular nature, it becomes quite easy to use the TSC comparator as components for fault-tolerant redundancy management, memory Built-In-Self-Test and CPU error detection caches in future SoC chip designs. With increasing density of logic gates in FPGAs following Moore's Law, it becomes highly practical to implement exhaustive online diagnosis through the proposed approach.

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