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Performance and analysis of Single-channel and Multiple channel based Approximate Distributed Arithmetic Filter Design

Santhosh Babu K C. Assistant Professor
Chirakshitha S, Eashanya K R , Eashanya K R , Ganavi A S ,Gowthami G
Dept of ECE, PESCE, Mandya

Abstract- — Efficient digital filtering is critical for modern signal processing applications. This work presents an Adaptive Distributed Arithmetic (ADA)-based FIR filter designed for single-channel and scalable multi-channel configurations on FPGA. The proposed design incorporates error- controlled approximation and optimized computation to reduce LUT usage, power consumption, and processing delay. Implementation using the Xilinx Vivado environment demonstrates improved area efficiency and speed while maintaining acceptable signal quality. The results indicate that the ADA approach is well- suited for low-power, high-throughput FPGA-based DSP applications.

Keywords— Adaptive Distributed Arithmetic (ADA), FIR filter, digital filtering, signal processing, FPGA implementation, multi-channel processing, single-channel design, Xilinx Vivado, LUT optimization, low power consumption, high throughput, area efficiency, processing delay reduction, error-controlled approximation, DSP applications.

I. INTRODUCTION

Digital Signal Processing (DSP) is widely used in applications such as communication, biomedical systems, and IoT, where efficient real-time filtering is essential. Finite Impulse Response (FIR) filters are preferred for their stability and predictable performance, but conventional implementations increase hardware complexity and power consumption. This work presents an Adaptive Distributed Arithmetic (ADA)-based FIR filter designed for efficient signal processing with reduced computational overhead. The proposed approach focuses on optimizing resource usage, minimizing power consumption, and maintaining acceptable signal quality. The design demonstrates improved efficiency and scalability, making it suitable for low-power, high-performance digital filtering applications.

II. LITERATURE SURVEY

[1]. Optimal Realization of Distributed Arithmetic-Based MAC Adaptive FIR Filter Architecture Incorporating Radix-4 and Radix-8 Computation (2024)
This work presents a Distributed Arithmetic-based adaptive FIR filter using radix-4 and radix-8 computation to improve efficiency and speed. It reduces multiplier dependency and enhances throughput. However, it does not address detailed single-channel and multi-channel approximate DA comparison on Artix-7 FPGA.

[2] "Delineation of Optimized Single and Multichannel Approximate DA-Based Filter Design Using Influential Single MAC Strategy for Trans-Multiplexer," 2024. This paper presents an approximate DA- based FIR filter using a single-MAC strategy for single and multichannel applications, improving area and speed. However, it lacks detailed FPGA-level analysis of power, SNR, and architectural trade-offs. This work addresses these gaps through a comprehensive comparison of MAC, DA, and ADA architectures.

[3] "Distributed Arithmetic-FIR Filter Design Using Approximate Karatsuba Multiplier and VLCSA," 2024.
This paper focuses on multiplier-less FIR filter implementation to reduce switching activity and power consumption using optimized coefficient representation and architectural modifications. Although it demonstrates improved energy efficiency, it does not consider approximate distributed arithmetic techniques with comparative analysis for single-channel and multi-channel configurations. In this work, such comparisons are carried out to evaluate performance across different architectures under identical conditions.

[4] "Energy Efficient FIR Filter Design Using Distributed Arithmetic," 2024.
This work presents an energy-efficient FIR filter using Distributed Arithmetic to reduce computational complexity. It shows that LUT-based implementation improves hardware efficiency. However, it does not analyze approximation effects such as signal quality and SNR, which are addressed in this work.

III. PROBLEM STATEMENT AND OBJECTIVES

FIR filter implementations on FPGA often face high resource usage, power consumption, and scalability limitations. Although conventional and DA-based designs address some issues, they still suffer from inefficient resource utilization and LUT growth. In addition, existing ADA methods lack thorough evaluation in terms of accuracy and scalability. Hence, an efficient, low-power, and scalable FIR filter design is required for real-time multi- channel processing.

1. To design and implement single- channel and multi-channel ADA- based FIR filter architectures.
2. To develop a scalable architecture supporting efficient multi-channel signal processing.
3. To evaluate performance in terms of area utilization, speed, power consumption, and latency.
4. To analyse the impact of approximation on signal quality using SNR and error metrics.

IV. DESIGN METHODOLOGY

The design methodology involves developing a 16-tap ADA-based FIR filter for single-channel and multi-channel configurations using VHDL. The architecture is designed with approximation techniques to reduce hardware complexity and is verified through simulation. Synthesis and implementation are performed in the Xilinx Vivado environment to evaluate resource utilization, timing, and power. The design is finally assessed based on area, speed, latency, and signal quality to ensure efficient and scalable performance.

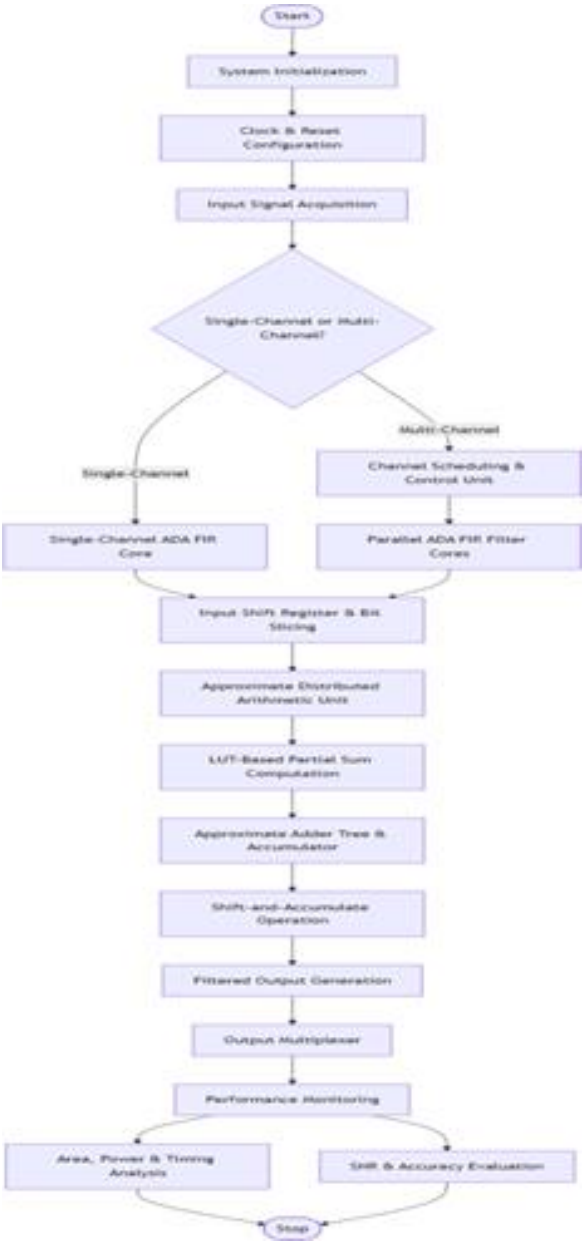

Figure 1 : Flowchart of the proposed ADA- based FIR filter operation

Block Diagram

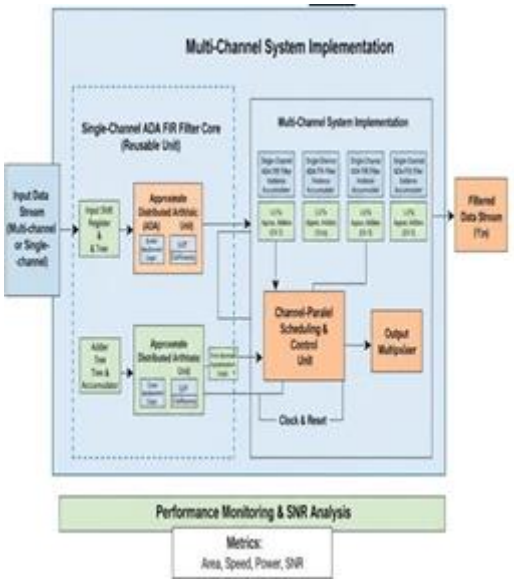

Figure 2 : Block diagram of the proposed multi-channel ADA-based FIR filter architecture

IV. RESULTS AND ANALYSIS

The results confirm that the proposed ADA- based FIR filter produces correct output responses for both single-channel and multi-channel configurations, as verified through simulation waveforms. The implementation demonstrates reduced hardware utilization due to optimized LUT and register usage, along with lower power consumption and improved operating speed. The use of approximation techniques achieves these improvements while maintaining acceptable signal quality, with minimal impact on accuracy. Overall, the analysis indicates that the ADA architecture provides an efficient and scalable solution for real-time digital filtering applications.

Single channel ADA :

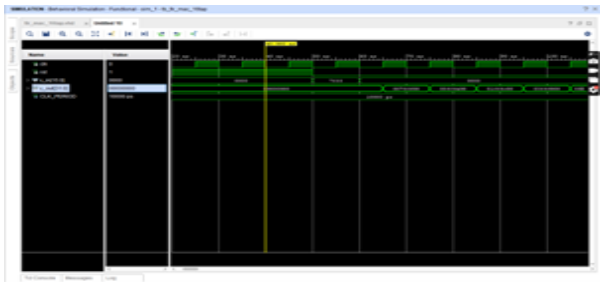

Figure 3: Simulation results of single- channel ADA FIR filter

Figure 4 : Power analysis (synthesis) of single-channel ADA FIR filter

Figure 5 : Power analysis (implementation) of single-channel ADA FIR filter

The multi-channel 16-tap FIR filter using Adaptive Distributed Arithmetic (ADA) demonstrates correct and synchronized operation across all channels, with valid outputs observed after pipeline delay. The design achieves efficient resource utilization with optimized LUT and register usage while eliminating DSP blocks. Implementation results show reduced power consumption and stable thermal behavior. Overall, the ADA architecture provides a scalable and efficient solution for real-time signal processing applications.

Multi – Channel ADA :

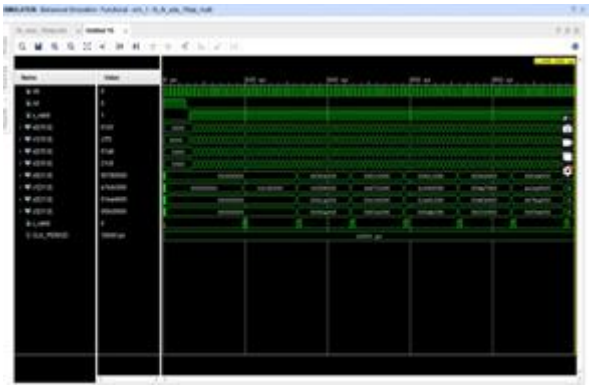

Figure 6: Simulation results of multi- channel ADA FIR filter

Figure 7: Power analysis (synthesis) of multi-channel ADA FIR filter

Figure 8 : Power analysis (implementation) of multi-channel ADA FIR filter

The multi-channel ADA-based 16-tap FIR filter shows correct and synchronized operation across all channels with valid outputs after pipeline delay. The design achieves efficient resource utilization with optimized LUT and register usage and no DSP blocks. Implementation results indicate reduced power consumption and stable thermal performance. Overall, the architecture provides a scalable and efficient solution for real-time signal processing applications.

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4. "Design and Implementation of Low Power Multiplierless FIR Filters on FPGA and ASIC," 2024.
5. "Energy Efficient FIR Filter Design Using Distributed Arithmetic," 2024.
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