International Journal of Scientific Research & Engineering Trends
Volume 1, Issue 3, May-2015, ISSN (Online): 2395-566X

Estimation of Progression Deviation of Dynamic RAM Memory Architecture

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***Abstract* – Some of the factors contributing to the variability increase are fundamental to the planar CMOS transistor architecture. Random dopant fluctuations (RDFs) and line-edge roughness (LER) are two examples of such intrinsic sources of variation. Other reasons for the variability increase are the advanced resolution-enhancement techniques (RETs) required to print lithography. New materials and performanceenhancement techniques add additional sources of variation. Finally, the transition to 300-mm wafers increases the impact of a cross-wafer non uniformity. This paper describes an efficient infrastructure for characterizing the various types of variation in transistor characteristics. A sample of results obtained from applying this infrastructure to a number of technologies at the 90nm, 65nm, and 45nm nodes is presented. This paper then illustrates the impact of the observed variability of DRAM along and digital circuit blocks used in system-on-chip designs. Different approaches for minimizing transistor variation and mitigating its impact on product performance and yield are also described.**
With this approach this will give the complete layout implementation of DRAM cell. From that it is also clear that the circuit which is design in schematic is having physical reliability as per as chip implementation is concern.

***Keywords* – Dynamic RAM, Memory Architecture, Line-Edge Roughness (LER), Random Dopant Fluctuations (RDFs), Resolution-Enhancement Techniques (RETs).**

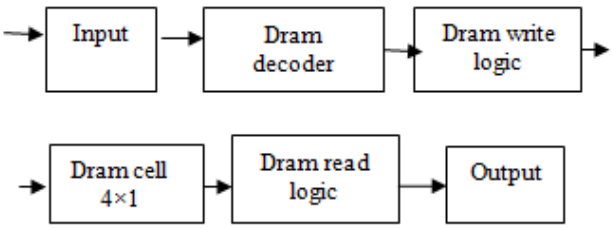
INTRODUCTION

VLSI design in the late CMOS era is driven by an ever-increasing challenge to cope with unreliable components at the device, circuit, and system levels. The impact of unreliability must be managed at various levels of the design abstraction. At the circuit, logic, micro architecture, and system levels, depending on the nature and degree of error manifestation starting at the physical level. This special issue addresses the problem of design for reliability at the 32-nm node and beyond, in the context of the emerging threat of progressively unreliable components used in VLSI chip design. Meanwhile, new research on efficient simulation and fault diagnosis techniques is receiving prominence in order to balance reliability challenges with other performance metrics.

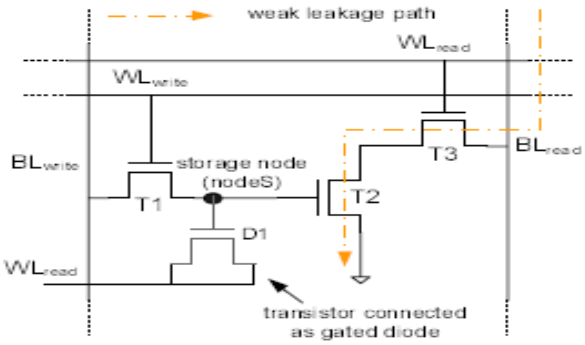
The situation is compounded by variations in line geometry that increase the failure probability. The scaling of CMOS transistors to nanometer-scale feature sizes is increasing the variability in transistor characteristics. This variability increase poses a challenge to the cost-effective utilization of scaled technologies. Meeting this challenge requires an efficient and comprehensive infrastructure for accurate characterization of the various types of variation. Accurate characterization forms the basis for variability minimization\and circuit design and layout techniques to reduce the impact of variation.

By considering the design variation into consideration paper giving the detail comparison between three node of technology 180nm, 130nm and 90nm with their sample result for DRAM complete cell, so it will be helpful to any researcher to consider this sample result for future work and also layout implementation.

ALGORITHEM & IMPLEMENTATION



Block diagram consist of above blocks DRAM decoder circuit is used to select the appropriate location which is followed by write logic to transfer the data then the main part of the circuit, that is DRAM cell which is actually responsible to hold the data , once it has been soared with the help of read logic we can read it.



The charge stored on the big capacitor of D1 boosts up the turn-on voltage of T2, rapidly discharging the bit line. As a result, the access speed can match the speed of 6T

SRAM cells. Conversely, when a "0" is stored, the capacitance of D1 is smaller and there is almost no voltage boosting, which keeps T2 off during the read. Hospice simulation results, shown in Figure, illustrate the operation of the 3T1D cell. The gate voltage of T2 is boosted by about 1.5-2.5 times (1.13V) the originally stored voltage (0.6V) if a "1" is stored when being read.

Although the speed of a 3T1D cell can be fast, this high-speed access is only valid for a limited time period after each write to the cell. This is because the charge on D1 leaks away over time. Figure 4 shows the relationship traditionally, the word "retention time" is defined as the time a DRAM cell can no longer hold the stored value.

Here DRAM decoder circuit is used to select appropriate location of DRAM which consist of 6 NMOS devices which work with the help of driver circuit which again consist of 20 MOS devices, these are compact design which lead in to minimum area requirement. To load the data in to memory there is a write logic which consist of 24 MOS devices, and also read logic consist of same devices. In order to check the performance of circuit when technology is change we are using different technology and find the certain conclusion regarding power consumption, area requirement and current consumption.

RESULTS

Output of Decoder Circuit Implemented in Schematic:

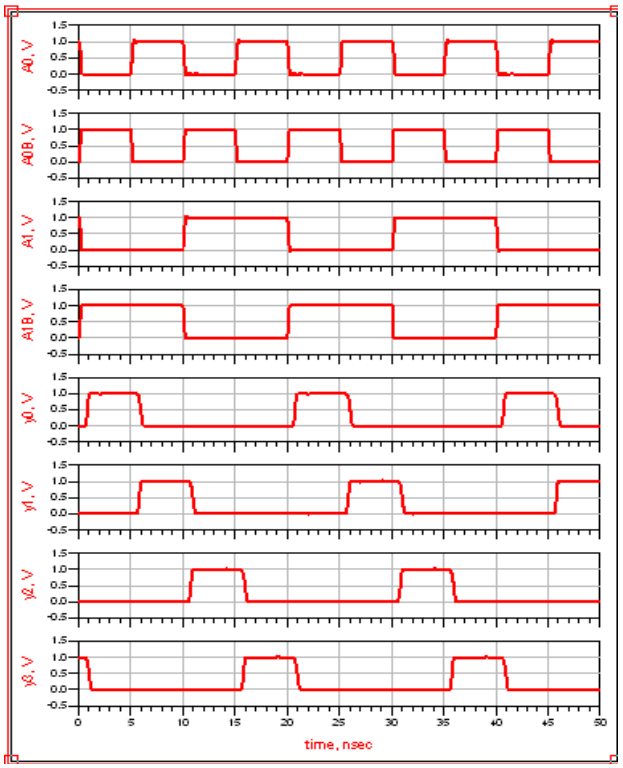


Fig.1. Output of decoder circuit (Schemetic)

As we have used decoder for selection of memory location of DRAM circuit this fig shows the output of decoder circuit.In this circuit is observed that when first clock and second clock is applied to active low then memory lacation Y0 is selected similarly it follows the following truth table.

Output of DRAM Cell of Schematic Structure

The output of DRAM circuit is as shown below it stoared in capacitor hence the peak value is in decreasing order. The capacitor are having the leakage but that are very less hence the appropriate level can get. As the data input is given to DRAM cell is 1100 it will stored this value in it.

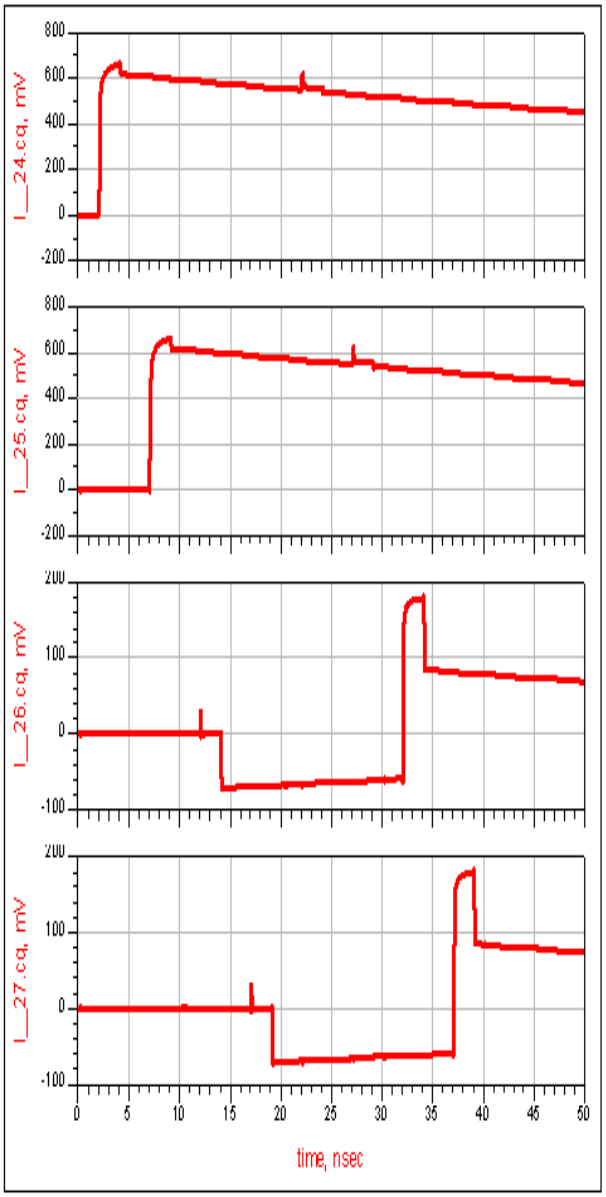


Fig.2. Output of DRAM cell of schematic structure

International Journal of Scientific Research & Engineering Trends
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VARIATION WITH TECHNOLOGY

Variability increase poses many difficult challenges for technology development. The most critical challenge is the development and adoption of variability-reduction methods. These range from techniques for robust transistor architecture and process integration options to the evaluation of process-control improvements. In addition to these technological challenges, the increase in variability necessitates modifications and improvements in the common technology-development methodologies. One such methodology is the use of split lots for technology optimization. In this approach, the technology is optimized for the target application through a series of DOE, where the goal of each experiment is to obtain incremental improvement in the technology characteristic of interest.

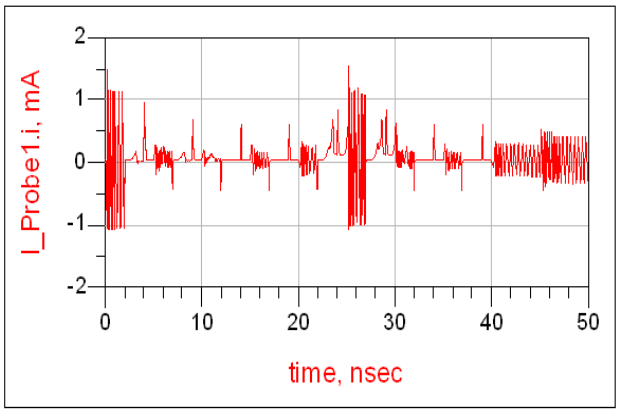

Fig.3. Current waveform of DRAM at 180nm technology

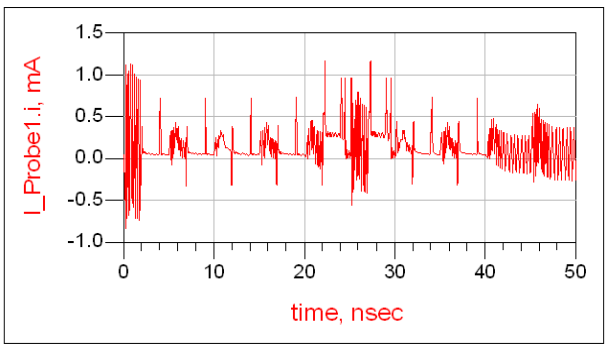

Fig.4. Current waveform of DRAM at 130nm technology

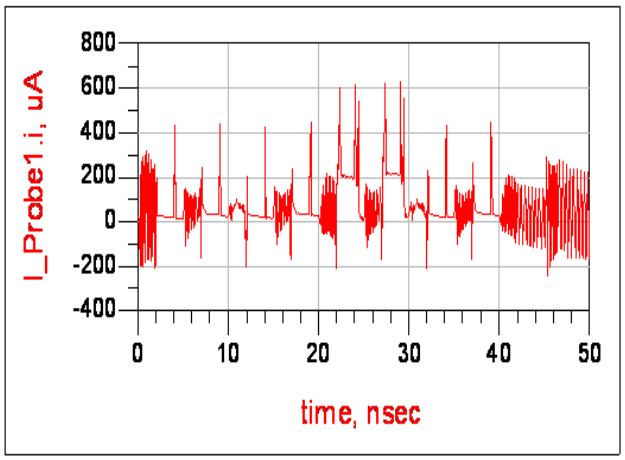

Fig.5. Current waveform a 90nm technology

As it is clear that the circuit is properly working hence now we will vary the same circuit with different technology which is most important part of this project. In this project we select three different node for variation 180nm, 130nm and 90nm. We are having sample result for the three different nodes of technology in term of power and area.

Above waveform are related to output current waveform at different nodes of technology Fig 4 shows the output current for 180nm technology it observed that the average current for that technology is 0.614 miliampere. Now when technology is reduced then the output current is reduces. From fig 5 the output current is 0.4628 miliampere for 130nm technology. When the output is taken for 90nm technology then the current is Average current is 0.21miliampere.

So from the discussion it is clear that when technology change then the current is reduces, it can be sample result for any researcher for their future work.

Now the area wise variation can be observed from the next discussion. In the following table all with different technology comparison is given in Table 1 detail comparison is given with 180nm technology, means all the required circuit is given in this Table 1 which shows the number of transistor required for DRAM, as technology used the area can be calculated, it is observed from the table the total area required is 34.2 micrometer[2].

Table 1: comparison of area required to DRAM with 180nm

Technology (Nanometer)	Circuits	PMOS	Area (µm2)	NMOS	Area (µm2)
180	Decoder	0	0	6	2.16
180	Decoder driver circuit	8	5.76	12	4.32
180	Write logic	12	8.64	12	4.32
180	DRAM cell (4×1)	0	0	16	17.28
180	Read logic	12	8.86	12	4.32
180	Buffer logic	2	3.6	2	1.8

From the following Table 2 it is clear that the total area required for DRAM in 130nm technology is 34.2 micrometer^2. It is observed that the technology is reduced the area is also reduces.

Table 2: comparison of area required to DRAM with 130nm

Technology (Nanometer)	Circuits	PMOS	Area (µm2)	NMOS	Area (µm2)
130	Decoder	0	0	6	1.17
130	Decoder driver circuit	8	3.12	12	2.34
130	Write logic	12	4.68	12	2.34
130	DRAM cell (4×1)	0	0	16	12.84
130	Read logic	12	4.68	12	2.34
130	Buffer logic	2	1.82	2	0.91

In 90nm technology the area again reduces it is observed that the area required for DRAM is 17.1 micrometer$^{2.}$. So we can say that as technology reduces the area also reduces

Table 3: comparison of area required to DRAM with 90nm

Technology (Nanometer)	Circuits	PMOS	Area (µm2)	NMOS	Area (µm2)
90	Decoder	0	0	6	1.08
90	Decoder driver circuit	8	2.88	12	2.16
90	Write logic	12	4.32	12	2.16
90	DRAM cell (4×1)	0	0	16	8.64
90	Read logic	12	4.32	12	2.16
90	Buffer logic	2	1.8	2	0.9

At last but not least we will compare all the parameter discusses up to in one glance so that we can finally take the conclusion. As following table indicate the detail comparison between various parameters with different technology. Row 1 indicate the node of technology, the second row indicate the supply voltage given to circuit. The next row will provide the current required for the technology for the same circuit. Which is followed by power required it is the most important characteristic of this project, and finally the last row indicate the total area required for that particular technology and we can also conclude that when technology changes then the parameter also change. This table indicates the sample results.

Table 4: Detail comparison of DRAM with different technology nodes

TECHNOLOGY (nanometer)	VOLTAGE (Volt)	CURRENT (milliamp)	POWER (milliwatt)	AREA (µm2)
180	1	0.614	0.614	34.2
130	1	0.4628	0.4628	34.2
90	1	0.21	0.21	17.1

CONCLUSION

The scaling of CMOS transistors to nanometer-scale feature sizes is increasing the variability in transistor characteristics. This variability increase poses a challenge to the cost-effective utilization of scaled technologies. Meeting this challenge requires an efficient and comprehensive infrastructure for accurate characterization of the various types of variation. Accurate characterization forms the basis for variability minimization and circuit design and layout techniques to reduce the impact of variation. This project presented our infrastructure for variability characterization along with a sample of results obtained from the application of this infrastructure to a number of 180, 130, and 90nm technologies.

Profitable utilization of scaled CMOS technologies requires techniques for variability minimization and robust circuit design and layout methods. Also provide the detail requirement of circuit with their area required with different technology. This project shows that as the technology reduces the power is reduce and also reduces the area.

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